Wireless Local Area Network (WLAN) Technology and Applications Including Techniques of Universal Frequency Translation

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This application claims priority to U.S. Provisional Application No. 60/147,129, filed August 4, 1999, which is incorporated by reference herein in its entirety

Cross-Reference to Other Applications

The following applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

"Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, Attorney Docket No. 1744.0010000, filed October 21, 1998, now U.S. Patent No. 6,061,551.

"Method and System for Down-Converting Electromagnetic Signals having Optimized Switch Structures," Ser. No. 09/293,095, Attorney Docket No. 1744.0010001, filed April 16, 1999.

"Method and System for Down-Converting Electromagnetic Signals Including Resonant Structures for Enhanced Energy Transfer," Ser. No. 09/293,342, Attorney Docket No. 1744.0010002, filed April 16, 1999.

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, Attorney Docket No. 1744.0020000, filed October 21, 1998, now U.S. Patent No. 6,091,940.

"Method and System for Frequency Up-Conversion with a Variety of Transmitter Configurations," Ser. No. 09/293,580, Attorney Docket No. 1744.0020002, filed April 16, 1999.

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, Attorney Docket No. 1744.0030000, filed October 21, 1998, now U.S. Patent No. 6,061,555.

"Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, Attorney Docket No. 1744.0130000, filed October 21, 1998, now U.S. Patent No. 6,049,706.

"Integrated Frequency Translation and Selectivity with a Variety of Filter Embodiments," Ser. No. 09/293,283, Attorney Docket No. 1744.0130001, filed April 16, 1999.

"Applications of Universal Frequency Translation," Ser. No. 09/261,129, Attorney Docket No. 1744.0140001, filed March 3, 1999.

"Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal, " Serial No. 09/525,615, Attorney Docket No. 1744.0450003, filed March 14, 2000.

"DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Serial No. 09/526,041, Attorney Docket No. 1744.0880000, filed March 14, 2000.

"Method and System for Down-converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships," Serial No. 09/550,644, Attorney Docket No. 1744.0010009, filed April 14, 2000.

"Wireless Local Area Network (WLAN) Using Universal Frequency Translation, " Serial No. (to be assigned), Attorney Docket No. 1744.0630001, filed August 4, 2000.

Background of the Invention

Field of the Invention

The present invention is generally related to frequency translation, and applications of same, such as, but not limited to wireless local area networks (WLANs).

Related Art

Various communication components exist for performing frequency down-conversion, frequency up-conversion, and filtering in the area of wireless local area networks (WLANs). Also, schemes exist for signal reception in the face of potential jamming signals.

Summary of the Invention

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. The drawing in which an element first appears is typically indicated by the leftmost character(s) and/or digit(s) in the corresponding reference number.

Brief Description of the Figures

The present invention will be described with reference to the accompanying drawings, wherein:

FIG. 1A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention.

FIG. 1B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention.

FIG. 1C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention.

FIG. 1D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

FIG. 2 is a block diagram of a universal frequency translation (UFT) module according to an alternative embodiment of the invention.

FIG. 3 is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

FIG. 4 is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

FIG. 5 is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention.

FIGS. 6A-6I illustrate example waveforms used to describe the operation of the UFU module.

FIG. 7 illustrates a UFT module used in a receiver according to an embodiment of the invention.

FIG. 8 illustrates a UFT module used in a transmitter according to an embodiment of the invention.

FIG. 9 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using a UFT module of the invention.

FIG. 10 illustrates a transceiver according to an embodiment of the invention.

FIG. 11 illustrates a transceiver according to an alternative embodiment of the invention.

FIG. 12 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention.

FIG. 13 illustrates a UFT module used in a unified down-conversion and filtering (UDF) module according to an embodiment of the invention.

FIG. 14 illustrates an example receiver implemented using a UDF module according to an embodiment of the invention.

FIGS. 15A-15F illustrate example applications of the UDF module according to embodiments of the invention.

FIG. 16 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention, wherein the receiver may be further implemented using one or more UFD modules of the invention.

FIG. 17 illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention.

FIG. 18 is a table of example values at nodes in the UDF module of FIG. 17.

FIG. 19 is a detailed diagram of an example UDF module according to an embodiment of the invention.

FIGS. 20A and 20G are example aliasing modules according to embodiments of the invention.

FIGS. 20B-20F are example waveforms used to describe the operation of the aliasing modules of FIGS. 20A and 20G.

FIG. 21 illustrates an enhanced signal reception system according to an embodiment of the invention.

FIGS. 22A-22F are example waveforms used to describe the system of FIG. 21.

FIG. 23A illustrates an example transmitter in an enhanced signal reception system according to an embodiment of the invention.

FIGS. 23B and 23C are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention.

FIG. 23D illustrates another example transmitter in an enhanced signal reception system according to an embodiment of the invention.

FIGS. 23E and 23F are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention.

FIG. 24A illustrates an example receiver in an enhanced signal reception system according to an embodiment of the invention.

FIGS. 24B-24J are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention.

FIG. 25 illustrates a block diagram of an example computer network.

FIG. 26 illustrates a block diagram of an example computer network.

FIG. 27 illustrates a block diagram of an example wireless interface.

FIG. 28 illustrates an example heterodyne implementation of the wireless interface illustrated in FIG. 27.

FIG. 29 illustrates an example in-phase/quadrature-phase (I/Q) heterodyne implementation of the interface illustrated in FIG. 27.

FIG. 30 illustrates an example high level block diagram of the interface illustrated in FIG. 27, in accordance with an embodiment of the present invention.

FIG. 31 illustrates a example block diagram of the interface illustrated in FIG. 29, in accordance with an embodiment of the invention.

FIG. 32 illustrates an example I/Q implementation of the interface illustrated in FIG.31.

FIGS. 33-38 illustrate example environments encompassed by embodiments of the invention.

FIG. 39 illustrates a block diagram of a WLAN interface according to an embodiment of the invention.

FIG. 40 illustrates a WLAN receiver according to an embodiment of the invention.

FIG. 41 illustrates a WLAN transmitter according to an embodiment of the invention.

FIGS. 42-44 are example implementations of a WLAN interface.

FIGS. 45, 46A, and 46B relate to an example MAC interface for an example WLAN interface embodiment.

FIGS. 47, 48, 49A, and 49B relate to an example demodulator/modulator facilitation module for an example WLAN interface embodiment.

FIGS. 50, 51, 52A, and 52B relate to an example alternate demodulator/modulator facilitation module for an example WLAN interface embodiment.

FIGS. 53 and 54 relate to an example receiver for an example WLAN interface embodiment.

FIGS. 55, 56A, and 56B relate to an example synthesizer for an example WLAN interface embodiment.

FIGS. 57, 58, 59, 60, 61A, and 61B relate to an example transmitter for an example WLAN interface embodiment.

FIGS. 62 and 63 relate to an example motherboard for an example WLAN interface embodiment.

FIGS. 64, 65, and 66 relate to example LNAs for an example WLAN interface embodiment.

FIGS. 67-68 illustrate example WLAN station configurations with hidden nodes.

FIG. 69 illustrates a general IEEE 802.11 frame format.

FIG. 70 illustrates a request to send frame.

FIG. 71A illustrates a transmitter according to embodiments of the present invention.

FIG. 71B illustrates an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. 71C illustrates an exemplary frequency spectrum for a harmonically rich signal that has multiple images that repeat at harmonics of the sampling frequency $1/T_S$, according to an embodiment of the present invention.

FIG. 71D illustrates an example embodiment of the modulator of FIG. 71B where the controlled switches in the UFT modules are field effect transistors (FET), according to an embodiment of the present invention.

FIG. 72A illustrates an exemplary clock signal.

FIGS 72B-72C illustrates exemplary control signals, according to embodiments of the present invention.

FIGs.72D-72I illustrate various example signal diagrams (vs. time) that are representative of an embodiment of the invention.

FIG. 72J depicts a frequency plot that graphically illustrates the effect of varying the sampling aperture of the control signals on the harmonically rich signal given a 200 MHZ harmonic clock, according to embodiments of the present invention.

FIG. 73A illustrates a transmitter that up-converts a baseband signal to an output signal having carrier insertion, according to an embodiment of the present invention.

FIG. 73B illustrates an exemplary frequency spectrum for a harmonically rich signal that has multiple harmonic images, according to an embodiment of the present invention.

FIG. 74 illustrates an I/Q transmitter with an in-phase (I) and quadrature (Q) configuration according to embodiments of the invention.

FIG. 75A depicts an exemplary frequency spectrum for the harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. 75B depicts an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG.75C illustrates an exemplary frequency spectrum for combined harmonically rich signal having images, according to an embodiment of the present invention.

FIG. 76A illustrates a transmitter that is a second embodiment for an I Q transmitter having a balanced configuration, according to an embodiment of the present invention.

FIG. 76B illustrates a transmitter, according to an embodiment of the present invention.

FIG. 77 illustrates a transmitter to provide any necessary carrier insertion by implementing a DC offset between the two sets of sampling UFT modules, according to an embodiment of the present invention.

FIG. 78 illustrates a transmitter that is a second embodiment of an I/Q transmitter having two DC terminals to cause DC offset, and therefore carrier insertion, according to an embodiment of the present invention.

FIG. 79A illustrates a universal transmitter that is a second embodiment of a universal transmitter having two balanced UFT modules in a shunt configuration, according to an embodiment of the present invention.

FIG. 79B illustrates an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. 79C illustrates an exemplary frequency spectrum for a harmonically rich signal that has multiple images that repeat at harmonics of the sampling frequency $1/T_S$, according to an embodiment of the present invention.

FIG. 79D illustrates an embodiment of the modulator of FIG. 79A, where the controlled switches in the UFT modules are field effect transistors (FET), according to the present invention.

FIG. 80 illustrates an I/Q transmitter embodiment, according to the present invention.

FIG. 81A depicts an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG. 81B depicts an exemplary frequency spectrum for a harmonically rich signal having harmonic images, according to an embodiment of the present invention.

FIG.81C illustrates an exemplary frequency spectrum for an I/Q harmonically rich signal having images, according to an embodiment of the present invention, according to an embodiment of the present invention.

FIG. 82 illustrates an I/Q transmitter having a balanced configuration, according to an embodiment of the present invention.

FIG.83 illustrates a transmitter, according to an embodiment of the present invention.

FIG. 84 shows a flowchart describing operation of the universal transmitter of FIG. 71A, according to an exemplary embodiment of the present invention.

FIG. 85 illustrates a flowchart describing operation of the balanced modulator of FIG. 71A, according to an exemplary embodiment of the present invention.

FIG. 86 illustrates a flowchart describing operation of the balanced modulator of FIG. 79A, according to an exemplary embodiment of the present invention.

FIG. 87 illustrates a flowchart describing operation of the balanced modulator and other components of FIG. 74, according to an exemplary embodiment of the present invention.

FIG. 88 illustrates a flowchart describing operation of the I/Q modulator of FIG. 80, according to an exemplary embodiment of the present invention.

FIGS. 89A-89E illustrate example embodiments for a pulse generator.

FIG. 90 illustrates an example clear to send frame.

FIG. 91 illustrates an example acknowledge (ACK) frame.

FIG. 92 illustrates an example data frame.

FIG. 93 illustrates an example information element.

FIG. 94 illustrates an example of the occurrence of multipath.

FIG. 95 illustrates an example graph showing delay spread versus symbol period.

FIG. 96 illustrates an exemplary channel impulse response.

FIG. 97 illustrates an exemplary WLAN cell.

FIG. 98 illustrates an example graph and equations related to path loss.

FIG. 99 illustrates an example graph providing a comparison of the theoretical Es/No vs Bit Error Rate (BER) curves for uncoded QPSK, PBCC 5.5-11 Mbps, CCK 5.5-11 Mbps, and Barker 1 and 2 Mbps.

FIG. 100 illustrates antenna diversity at the access point (AP).

FIG. 101A illustrates an IBSS with mobile stations that communicate through an AP.

FIG. 101B illustrates an AP 10102 that includes a universal frequency translation module.

FIG. 102 is an example PCMCIA test bed assembly for a WLAN interface according to an embodiment of the invention.

FIG. 103 illustrates an exemplary I/Q modulation receiver, according to an embodiment of the present invention.

FIG. 104 illustrates a I/Q modulation control signal generator, according to an embodiment of the present invention.

FIG. 105 illustrates example waveforms related to the I/Q modulation control signal generator of FIG. 104.

FIG. 106 illustrates example control signal waveforms overlaid upon an input RF signal.

FIG. 107 illustrates a I/Q modulation receiver circuit diagram, according to an embodiment of the present invention.

FIGS. 108-118 illustrate example waveforms related to the receiver of FIG. 107.

FIG. 119 illustrates a single channel receiver, according to an embodiment of the present invention.

FIG. 120 illustrates some aspects of charge injection related to embodiments of the present invention.

FIG. 121 illustrates an exemplary circuit configuration for reducing DC offset voltage caused by charge injection, according to an embodiment of the present invention.

FIG. 122 depicts a flowchart that illustrates operational steps for down-converting an input signal and reducing a DC offset voltage, according to an embodiment of the present invention.

FIG. 123 depicts a flowchart that illustrates operational steps for down-converting a RF I/Q modulated signal and reducing DC offset voltages, according to an embodiment of the present invention.

FIG. 124 illustrates an example IBSS with mobile stations that must be in direct communication range to communicate with each other.

FIG. 125 illustrates an exemplary ESS.

FIG. 126 illustrates a state diagram showing the relationship between state variables and services.

FIG. 127 illustrates a station moving between APs.

FIG. 128A illustrates an OSI model including a PHY layer.

FIGS. 128B-128D illustrate exemplary block diagrams of PMD sublayers incorporating universal frequency translation technology, according to embodiments of the present invention.

FIG. 129A illustrates an exemplary DSSS PMD transmitter.

FIG. 129B illustrates an exemplary DSSS PMD receiver.

FIG. 129C illustrates an exemplary block diagrams of a DPSK modulation mode transmitter, according to an embodiment of the present invention.

FIGS.129D-129F illustrate exemplary block diagrams related to DBPSK modulation mode transmitters, according to embodiments of the present invention.

FIGS.129G-129I illustrate exemplary block diagrams related to DQPSK modulation mode transmitters, according to embodiments of the present invention.

FIG. 129J illustrates an exemplary block diagrams of a DBPSK/DQPSK modulation mode receiver, according to an embodiment of the present invention.

FIG. 129K illustrates an exemplary block diagram of a de-spread correlator and a DBPSK/DQPSK demodulator sharing components, according to embodiments of the present invention.

FIG. 129L illustrates an exemplary block diagram of a receiver DSSS PMD, according to an embodiment of the present invention.

FIGS.129M-129P illustrate exemplary block diagrams related to DBPSK modulation mode receivers, according to embodiments of the present invention.

FIGS.129Q-129S illustrate exemplary block diagrams related to DQPSK modulation mode transmitters, according to embodiments of the present invention.

FIG. 130 illustrates a PPDU frame.

FIG. 131 illustrates constellation patterns related to DBPSK and DQPSK modulation.

FIG. 132A illustrates application of an 11-bit Barker word and information bits to a modulo-2 adder (XOR function).

FIGS. 132B-132E illustrate transmitter and receiver signals before and after spreading.

FIG. 133 illustrates a filtered SinX/X function.

FIG. 134 illustrates a DSSS channel arrangement for North America.

FIGS. 135A and 135B illustrate block diagrams showing elements of the FHSS PMD transmitter and receiver, respectively.

FIG. 135C illustrates an exemplary block diagram of a 2-level/4-level GFSK modulator, according to an embodiment of the present invention.

FIGS.135D-135E illustrate exemplary block diagrams related to the 2-level/4-level GFSK modulator of FIG. 135C, according to embodiments of the present invention.

FIG. 135F illustrates an exemplary block diagram of a 2-level/4-level GFSK demodulator, according to an embodiment of the present invention.

FIG.135G illustrates an exemplary block diagrams related to the 2-level/4-level GFSK modulator of FIG. 135F, according to an embodiment of the present invention.

FIG. 136 illustrates a PLCP protocol data unit (PPDU) related to a DSSS PHY.

FIG. 137 illustrates a block diagram of an exemplary IR PMD sublayer.

FIG. 138 illustrates a PPDU related to an IR PHY.

FIG. 139 illustrates a PPDU related to an OFDM PHY.

FIGS. 140A and 140B illustrate exemplary block diagrams of an IEEE 802.11a OFDM PMD transmitter and receiver, respectively.

FIGS. 140C illustrates an exemplary PSK/QAM modulator, according to an embodiment of the present invention.

FIGS.140D-140E illustrate exemplary block diagrams for transmitting BPSK modulated signals related to the PSK/QAM modulator of FIG. 140C, according to embodiments of the present invention.

FIGS.140F-140H illustrate exemplary block diagrams for transmitting QAM modulated signals related to the PSK/QAM modulator of FIG. 140C, according to embodiments of the present invention.

FIGS. 140I illustrates an exemplary PSK/QAM demodulator, according to an embodiment of the present invention.

FIG.140J illustrates an exemplary block diagram for receiving BPSK modulated signals related to the PSK/QAM demodulator of FIG. 140I, according to an embodiment of the present invention.

FIGS.140K-140L illustrate exemplary block diagrams for receiving QPSK/QAM modulated signals related to the PSK/QAM demodulator of FIG. 140I, according to embodiments of the present invention.

FIG. 141A illustrates a PPDU with a long PLCP preamble.

FIG. 141B illustrates a PPDU with a short preamble.

FIG. 142 illustrates an example of a typical HR/DSSS channel arrangement for non-interfering channels for North America.

FIG. 143A illustrates an exemplary transmit HR/DSSS PMD, according to an embodiment of the present invention.

FIG. 143B illustrates an exemplary block diagram for a CCK modulator.

FIGS. 144A and 144B illustrate use of scrambled binary bits of the PSDU for 5.5 Mbps and 11 Mbps operation.

FIG. 145A illustrates an exemplary PBCC modulator.

FIG. 145B illustrates a receiver HR/DSSS PMD, according to an embodiment of the present invention.

FIG. 145C illustrates a receiver HR/DSSS PMD that includes a CCK demodulator, according to an embodiment of the present invention.

FIG. 145D illustrates a receiver HR/DSSS PMD that includes a PBCC demodulator, according to an embodiment of the present invention.

FIGS. 146 to 212 illustrate schematics showing an integrated circuit implementation of an exemplary embodiment of the present invention.

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Detailed Description of the Preferred Embodiments

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1. Universal Frequency Translation

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

FIG. 1A illustrates a universal frequency translation (UFT) module 102 according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

As indicated by the example of FIG. 1A, some embodiments of the UFT module 102 include three ports (nodes), designated in FIG. 1A as Port 1, Port 2, and Port 3. Other UFT embodiments include other than three ports.

Generally, the UFT module 102 (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module 102 (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

An example embodiment of the UFT module 103 is generally illustrated in FIG. 1B. Generally, the UFT module 103 includes a switch 106 controlled by a control signal 108. The switch 106 is said to be a controlled switch.

As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. 2 illustrates an example UFT module 202. The example UFT module 202 includes a diode 204 having two ports, designated as Port 1 and Port 2/3. This embodiment does not include a third port, as indicated by the dotted line around the "Port 3" label.

The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

For example, a UFT module 115 can be used in a universal frequency down-conversion (UFD) module 114, an example of which is shown in FIG. 1C. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal.

As another example, as shown in FIG. 1D, a UFT module 117 can be used in a universal frequency up-conversion (UFU) module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal.

These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on

the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

2. *Frequency Down-Conversion*

The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998, the full disclosure of which is incorporated herein by reference, as well as other applications cited above. A relevant portion of the above mentioned patent application is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal.

FIG. 20A illustrates an aliasing module 2000 (also called a universal frequency down-conversion module) for down-conversion using a universal frequency translation (UFT) module 2002 which down-converts an EM input signal 2004. In particular embodiments, aliasing module 2000 includes a switch 2008 and a capacitor 2010. The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch 2008 is in series with input signal 2004 and capacitor 2010 is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. 20G), the capacitor 2010 is in series with the input signal 2004 and the switch 2008 is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module 2000 with UFT module 2002 can be easily tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal 2004.

In one implementation, aliasing module 2000 down-converts the input signal 2004 to an intermediate frequency (IF) signal. In another implementation, the aliasing module 2000 down-

converts the input signal 2004 to a demodulated baseband signal. In yet another implementation, the input signal 2004 is a frequency modulated (FM) signal, and the aliasing module 2000 down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

In an embodiment, the control signal 2006 includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal 2004. In this embodiment, the control signal 2006 is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal 2004. Preferably, the frequency of control signal 2006 is much less than the input signal 2004.

A train of pulses 2018 as shown in FIG. 20D controls the switch 2008 to alias the input signal 2004 with the control signal 2006 to generate a down-converted output signal 2012. More specifically, in an embodiment, switch 2008 closes on a first edge of each pulse 2020 of FIG. 20D and opens on a second edge of each pulse. When the switch 2008 is closed, the input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal to the capacitor 2010. The charge stored during successive pulses forms down-converted output signal 2012.

Exemplary waveforms are shown in FIGS. 20B-20F.

FIG. 20B illustrates an analog amplitude modulated (AM) carrier signal 2014 that is an example of input signal 2004. For illustrative purposes, in FIG. 20C, an analog AM carrier signal portion 2016 illustrates a portion of the analog AM carrier signal 2014 on an expanded time scale. The analog AM carrier signal portion 2016 illustrates the analog AM carrier signal 2014 from time t_0 to time t_1.

FIG. 20D illustrates an exemplary aliasing signal 2018 that is an example of control signal 2006. Aliasing signal 2018 is on approximately the same time scale as the analog AM carrier signal portion 2016. In the example shown in FIG. 20D, the aliasing signal 2018 includes a train of pulses 2020 having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses 2020 repeat at an aliasing rate, or pulse

repetition rate of aliasing signal 2018. The aliasing rate is determined as described below, and further described in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998.

As noted above, the train of pulses 2020 (i.e., control signal 2006) control the switch 2008 to alias the analog AM carrier signal 2016 (i.e., input signal 2004) at the aliasing rate of the aliasing signal 2018. Specifically, in this embodiment, the switch 2008 closes on a first edge of each pulse and opens on a second edge of each pulse. When the switch 2008 is closed, input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal 2004 to the capacitor 2010. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples 2022 form down-converted signal portion 2024 (FIG. 20E) that corresponds to the analog AM carrier signal portion 2016 (FIG. 20C) and the train of pulses 2020 (FIG. 20D). The charge stored during successive under-samples of AM carrier signal 2014 form the down-converted signal 2024 (FIG. 20E) that is an example of down-converted output signal 2012 (FIG. 20A). In FIG. 20F, a demodulated baseband signal 2026 represents the demodulated baseband signal 2024 after filtering on a compressed time scale. As illustrated, down-converted signal 2026 has substantially the same "amplitude envelope" as AM carrier signal 2014. Therefore, FIGS. 20B-20F illustrate down-conversion of AM carrier signal 2014.

The waveforms shown in FIGS. 20B-20F are discussed herein for illustrative purposes only, and are not limiting. Additional exemplary time domain and frequency domain drawings, and exemplary methods and systems of the invention relating thereto, are disclosed in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998.

The aliasing rate of control signal 2006 determines whether the input signal 2004 is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal 2004, the aliasing rate of the control signal 2006, and the down-converted output signal 2012 are illustrated below:

(Freq. of input signal 2004) = n•(Freq. of control signal 2006) ± (Freq. of down-converted output signal 2012)

For the examples contained herein, only the "+" condition will be discussed. The value of n represents a harmonic or sub-harmonic of input signal 2004 (e.g., $n = 0.5, 1, 2, 3, \ldots$).

When the aliasing rate of control signal 2006 is off-set from the frequency of input signal 2004, or off-set from a harmonic or sub-harmonic thereof, input signal 2004 is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal 2004. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal 2006 would be calculated as follows:

$$(Freq_{input} - Freq_{IF})/n = Freq_{control}$$
$$(901\ MHZ - 1\ MHZ)/n = 900/n$$

For $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 would be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating down-conversion of analog and digital AM, PM and FM signals to IF signals, and exemplary methods and systems thereof, are disclosed in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998.

Alternatively, when the aliasing rate of the control signal 2006 is substantially equal to the frequency of the input signal 2004, or substantially equal to a harmonic or sub-harmonic thereof, input signal 2004 is directly down-converted to a demodulated baseband signal. This is because,

without modulation, the under-sampling pulses occur at the same point of subsequent cycles of the input signal 2004. As a result, the under-samples form a constant output baseband signal. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHZ input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal 2006 would be calculated as follows:

$$(Freq_{input} - Freq_{IF})/n = Freq_{control}$$
$$(900\ MHZ - 0\ MHZ)/n = 900\ MHZ/n$$

For $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating direct down-conversion of analog and digital AM and PM signals to demodulated baseband signals, and exemplary methods and systems thereof, are disclosed in the U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998.

Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1 + F_2) \div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal 2006 would be calculated as follows:

$$\text{Frequency of the input} = (F_1 + F_2) \div 2$$
$$= (899\ MHZ + 901\ MHZ) \div 2$$

= 900 MHZ

Frequency of the down-converted signal = 0 (i.e., baseband)

$$(Freq_{input} - Freq_{IF})/n = Freq_{control}$$
$$(900\ MHZ - 0\ MHZ)/n = 900\ MHZ/n$$

For $n = 0.5, 1, 2, 3$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2.

As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHZ and F_2 equal to 901 MHZ, to an ASK signal, the aliasing rate of the control signal 2006 should be substantially equal to:

$$(900\ MHZ - 0\ MHZ)/n = 900\ MHZ/n, \text{ or}$$
$$(901\ MHZ - 0\ MHZ)/n = 901\ MHZ/n.$$

For the former case of 900 MHZ/n, and for $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. For the latter case of 901 MHZ/n, and for $n = 0.5, 1, 2, 3, 4$, etc., the frequency of the control signal 2006 should be substantially equal to 1.802 GHz, 901 MHZ, 450.5 MHZ, 300.333 MHZ, 225.25 MHZ, etc. The frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHZ).

Exemplary time domain and frequency domain drawings, illustrating down-conversion of FM signals to non-FM signals, and exemplary methods and systems thereof, are disclosed in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998.

In an embodiment, the pulses of the control signal 2006 have negligible apertures that tend towards zero. This makes the UFT module 2002 a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

In another embodiment, the pulses of the control signal 2006 have non-negligible apertures that tend away from zero. This makes the UFT module 2002 a lower input impedance device. This allows the lower input impedance of the UFT module 2002 to be substantially matched with a source impedance of the input signal 2004. This also improves the energy transfer from the input signal 2004 to the down-converted output signal 2012, and hence the efficiency and signal to noise (s/n) ratio of UFT module 2002.

Exemplary systems and methods for generating and optimizing the control signal 2006, and for otherwise improving energy transfer and s/n ratio, are disclosed in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998.

2.1 Charge Injection Reduction Embodiment

In this section, an embodiment, according to the present invention, is provided for reducing or eliminating DC offset due at least to charge injection. FIG. 120 illustrates some aspects of charge injection related to the present invention. FIG. 120 shows a UFD module 12000 comprising a UFT module 12002, a storage device 12004, and a reference potential 12006. In an embodiment, UFT module 12002 comprises a MOSFET 12008, and storage device 12004 comprises a capacitor 12010, although the invention is not limited to this example.

An input RF signal 12014 is received by a first terminal 12028 of MOSFET 12008. A control signal 12018 is received by a second terminal 12030 of MOSFET 12008. A third terminal 12032 of MOSFET 12008 is coupled to a first terminal 12034 of storage device 12004. A second terminal 12036 of storage device 12004 is coupled to reference potential 12006 such as a ground 12012, or some other potential. In an embodiment, MOSFET 12008 contained within UFT module 12002 opens and closes as a function of control signal 12018. As a result of the opening and closing of this switch, a down-converted signal, referred to as output signal 12016, results.

A well known phenomenon called charge injection may occur in such a switching environment. As control signal 12018 applies a pulse waveform to the gate of MOSFET 12008, MOSFET 12008 is caused to open and close. During this operation, charge allowed to flow along a DC path 12024 may build on the gate-to-drain and/or gate-to-source junctions of MOSFET 12008, as indicated on FIG. 120 as charge buildup 12020 (note that the source and drain terminals of MOSFET 12008 are essentially interchangeable). Charge buildup 12020 may leak from MOSFET 12008 through leakage path 12022, and become stored on capacitor 12010. This charge that becomes stored on capacitor 12010 may cause a change in the voltage across capacitor 12010. This voltage change may accordingly appear on output signal 12016 as a potentially non-negligible DC offset voltage. This non-negligible DC offset voltage on output signal 12016 may lead to difficulties in recovering the baseband information content of output signal 12016. Hence, it would be advantageous to reduce or prevent this potential generation of DC offset voltage caused by this interaction of control signal 12018 with UFD module 12000.

FIG. 121 illustrates an exemplary circuit configuration for reducing unwanted DC offset voltage caused by charge injection, according to an embodiment of the present invention.

FIG. 121 shows UFD module 12000 of FIG. 120, with a capacitor 12126 coupled between input RF signal 12014 and UFD module 12000. Capacitor 12126 is preferably a small valued capacitor, such as, but not limited to, 10 pF. The value for capacitor 12126 will vary depending upon the application, and accordingly its characteristics are implementation and application specific. Capacitor 12126 prevents DC current from flowing along the path shown as DC path 12024 in FIG.

120, and thus reduces or prevents the flow of charge to, and build up of charge on capacitor 12010. This in turn reduces or prevents a DC offset voltage resulting from the above described charge injection from appearing on output signal 12016. Hence, the baseband information content of output signal 12016 may be more accurately ascertained.

FIG. 122 depicts a flowchart 12200 that illustrates operational steps corresponding to FIG. 121, for down-converting an input signal and reducing a DC offset voltage, according to an embodiment of the present invention. The invention is not limited to this operational description. Rather, it will be apparent to persons skilled in the relevant art(s) from the teachings herein that other operational control flows are within the scope and spirit of the present invention. It is noted that the ordering of steps is flexible, and not limited to that shown in the flowcharts, and described herein. In the following discussion, the steps in FIG. 122 will be described.

In step 12202, an input signal is coupled by a series capacitor to an input of a universal frequency down-conversion module.

In step 12204, the input signal is frequency down-converted with the universal frequency down-conversion module to a down-converted signal. The input signal is down-converted according to a control signal. The control signal under-samples the input signal.

In step 12206, a DC offset voltage in the down-converted signal generated during step 12204 is reduced. In an embodiment, the DC offset voltage is generated at least by charge injection effects due to interaction of the control signal with the universal frequency down-conversion module, as further described above.

It should be understood that the above examples are provided for illustrative purposes only. The invention is not limited to this embodiment. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

2.2 Example I/Q Modulation Receiver Embodiments

FIG. 103 illustrates an exemplary I/Q modulation receiver 10300, according to an embodiment of the present invention. I/Q modulation receiver 10300 has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation.

I/Q modulation receiver 10300 comprises a first UFD module 10302, a first optional filter 10304, a second UFD module 10306, a second optional filter 10308, a third UFD module 10310, a third optional filter 10312, a fourth UFD module 10314, a fourth filter 10316, an optional LNA 10318, a first differential amplifier 10320, a second differential amplifier 10322, and an antenna 10372.

I/Q modulation receiver 10300 receives, down-converts, and demodulates a I/Q modulated RF input signal 10382 to an I baseband output signal 10384, and a Q baseband output signal 10386. I/Q modulated RF input signal comprises a first information signal and a second information signal that are I/Q modulated onto an RF carrier signal. I baseband output signal 10384 comprises the first baseband information signal. Q baseband output signal 10386 comprises the second baseband information signal.

Antenna 10372 receives I/Q modulated RF input signal 10382. I/Q modulated RF input signal 10382 is output by antenna 10372 and received by optional LNA 10318. When present, LNA 10318 amplifies I/Q modulated RF input signal 10382, and outputs amplified I/Q signal 10388.

First UFD module 10302 receives amplified I/Q signal 10388. First UFD module 10302 down-converts the I-phase signal portion of amplified input I/Q signal 10388 according to an I control signal 10390. First UFD module 10302 outputs an I output signal 10398.

In an embodiment, first UFD module 10302 comprises a first storage module 10324, a first UFT module 10326, and a first voltage reference 10328. In an embodiment, a switch contained within first UFT module 10326 opens and closes as a function of I control signal 10390. As a result of the opening and closing of this switch, which respectively couples and de-couples first storage module 10324 to and from first voltage reference 10328, a down-converted signal, referred to as I

output signal 10398, results. First voltage reference 10328 may be any reference voltage, and is preferably ground. I output signal 10398 is stored by first storage module 10324.

In a preferred embodiment, first storage module 10324 comprises a first capacitor 10374. In addition to storing I output signal 10398, first capacitor 10374 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on I output signal 10398, in a similar fashion to that of capacitor 12126 shown in FIG. 121. Refer to Section 2.1 above for further discussion on reducing or eliminating charge injection with a series capacitor such as capacitor 12126.

I output signal 10398 is received by optional first filter 10304. When present, first filter 10304 is a high pass filter to at least filter I output signal 10398 to remove any carrier signal "bleed through". In a preferred embodiment, when present, first filter 10304 comprises a first resistor 10330, a first filter capacitor 10332, and a first filter voltage reference 10334. Preferably, first resistor 10330 is coupled between I output signal 10398 and a filtered I output signal 10307, and first filter capacitor 10332 is coupled between filtered I output signal 10307 and first filter voltage reference 10334. Alternately, first filter 10304 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). First filter 10304 outputs filtered I output signal 10307.

Second UFD module 10306 receives amplified I/Q signal 10388. Second UFD module 10306 down-converts the inverted I-phase signal portion of amplified input I/Q signal 10388 according to an inverted I control signal 10392. Second UFD module 10306 outputs an inverted I output signal 10301.

In an embodiment, second UFD module 10306 comprises a second storage module 10336, a second UFT module 10338, and a second voltage reference 10340. In an embodiment, a switch contained within second UFT module 10338 opens and closes as a function of inverted I control signal 10392. As a result of the opening and closing of this switch, which respectively couples and de-couples second storage module 10336 to and from second voltage reference 10340, a down-converted signal, referred to as inverted I output signal 10301, results. Second voltage reference

10340 may be any reference voltage, and is preferably ground. Inverted I output signal 10301 is stored by second storage module 10336.

In a preferred embodiment, second storage module 10336 comprises a second capacitor 10376. In addition to storing inverted I output signal 10301, second capacitor 10376 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted I output signal 10301, in a similar fashion to that of capacitor 12126 shown in FIG. 121. Refer to Section 2.1 above for further discussion on reducing or eliminating charge injection with a series capacitor such as capacitor 12126.

Inverted I output signal 10301 is received by optional second filter 10308. When present, second filter 10308 is a high pass filter to at least filter inverted I output signal 10301 to remove any carrier signal "bleed through". In a preferred embodiment, when present, second filter 10308 comprises a second resistor 10342, a second filter capacitor 10344, and a second filter voltage reference 10346. Preferably, second resistor 10342 is coupled between inverted I output signal 10301 and a filtered inverted I output signal 10309, and second filter capacitor 10344 is coupled between filtered inverted I output signal 10309 and second filter voltage reference 10346. Alternately, second filter 10308 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Second filter 10308 outputs filtered inverted I output signal 10309.

First differential amplifier 10320 receives filtered I output signal 10307 at its non-inverting input and receives filtered inverted I output signal 10309 at its inverting input. First differential amplifier 10320 subtracts filtered inverted I output signal 10309 from filtered I output signal 10307, amplifies the result, and outputs I baseband output signal 10384. Other suitable subtractor and/or amplification modules may be substituted for first differential amplifier 10320, and second differential amplifier 10322, as would be understood by persons skilled in the relevant art(s) from the teachings herein. Because filtered inverted I output signal 10309 is substantially equal to an inverted version of filtered I output signal 10307, I baseband output signal 10384 is substantially equal to filtered I output signal 10309, with its amplitude doubled. Furthermore, filtered I output

signal 10307 and filtered inverted I output signal 10309 may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including first UFD module 10302 and second UFD module 10306, respectively. When first differential amplifier 10320 subtracts filtered inverted I output signal 10309 from filtered I output signal 10307, these noise and DC offset contributions substantially cancel each other.

Third UFD module 10310 receives amplified I/Q signal 10388. Third UFD module 10310 down-converts the Q-phase signal portion of amplified input I/Q signal 10388 according to an Q control signal 10394. Third UFD module 10310 outputs an Q output signal 10303.

In an embodiment, third UFD module 10310 comprises a third storage module 10348, a third UFT module 10350, and a third voltage reference 10352. In an embodiment, a switch contained within third UFT module 10350 opens and closes as a function of Q control signal 10394. As a result of the opening and closing of this switch, which respectively couples and de-couples third storage module 10348 to and from third voltage reference 10352, a down-converted signal, referred to as Q output signal 10303, results. Third voltage reference 10352 may be any reference voltage, and is preferably ground. Q output signal 10303 is stored by third storage module 10348.

In a preferred embodiment, third storage module 10348 comprises a third capacitor 10378. In addition to storing Q output signal 10303, third capacitor 10378 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on Q output signal 10303, in a similar fashion to that of capacitor 12126 shown in FIG. 121. Refer to Section 2.1 above for further discussion on reducing or eliminating charge injection with a series capacitor such as capacitor 12126.

Q output signal 10303 is received by optional third filter 10312. When present, third filter 10312 is a high pass filter to at least filter Q output signal 10303 to remove any carrier signal "bleed through". In a preferred embodiment, when present, third filter 10312 comprises a third resistor 10354, a third filter capacitor 10358, and a third filter voltage reference 10358. Preferably, third resistor 10354 is coupled between Q output signal 10303 and a filtered Q output signal 10311, and third filter capacitor 10356 is coupled between filtered Q output signal 10311 and third filter voltage

reference 10358. Alternately, third filter 10312 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Third filter 10312 outputs filtered Q output signal 10311.

Fourth UFD module 10314 receives amplified I/Q signal 10388. Fourth UFD module 10314 down-converts the inverted Q-phase signal portion of amplified input I/Q signal 10388 according to an inverted Q control signal 10396. Fourth UFD module 10314 outputs an inverted Q output signal 10305.

In an embodiment, fourth UFD module 10314 comprises a fourth storage module 10360, a fourth UFT module 10362, and a fourth voltage reference 10364. In an embodiment, a switch contained within fourth UFT module 10362 opens and closes as a function of inverted Q control signal 10396. As a result of the opening and closing of this switch, which respectively couples and de-couples fourth storage module 10360 to and from fourth voltage reference 10364, a down-converted signal, referred to as inverted Q output signal 10305, results. Fourth voltage reference 10364 may be any reference voltage, and is preferably ground. Inverted Q output signal 10305 is stored by fourth storage module 10360.

In a preferred embodiment, fourth storage module 10360 comprises a fourth capacitor 10380. In addition to storing inverted Q output signal 10305, fourth capacitor 10380 reduces or prevents a DC offset voltage resulting from above described charge injection from appearing on inverted Q output signal 10305, in a similar fashion to that of capacitor 12126 shown in FIG. 121. Refer to Section 2.1 above for further discussion on reducing or eliminating charge injection with a series capacitor such as capacitor 12126.

Inverted Q output signal 10305 is received by optional fourth filter 10316. When present, fourth filter 10316 is a high pass filter to at least filter inverted Q output signal 10305 to remove any carrier signal "bleed through". In a preferred embodiment, when present, fourth filter 10316 comprises a fourth resistor 10366, a fourth filter capacitor 10368, and a fourth filter voltage reference 10370. Preferably, fourth resistor 10366 is coupled between inverted Q output signal 10305 and a filtered inverted Q output signal 10313, and fourth filter capacitor 10368 is coupled between filtered

inverted Q output signal 10313 and fourth filter voltage reference 10370. Alternately, fourth filter 10316 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Fourth filter 10316 outputs filtered inverted Q output signal 10313.

Second differential amplifier 10322 receives filtered Q output signal 10311 at its non-inverting input and receives filtered inverted Q output signal 10313 at its inverting input. Second differential amplifier 10322 subtracts filtered inverted Q output signal 10313 from filtered Q output signal 10311, amplifies the result, and outputs Q baseband output signal 10386. Because filtered inverted Q output signal 10313 is substantially equal to an inverted version of filtered Q output signal 10311, Q baseband output signal 10386 is substantially equal to filtered Q output signal 10313, with its amplitude doubled. Furthermore, filtered Q output signal 10311 and filtered inverted Q output signal 10313 may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including third UFD module 10310 and fourth UFD module 10314, respectively. When second differential amplifier 10322 subtracts filtered inverted Q output signal 10313 from filtered Q output signal 10311, these noise and DC offset contributions substantially cancel each other.

FIG. 123 depicts a flowchart 12300 that illustrates operational steps corresponding to FIG. 103, for down-converting a RF I/Q modulated signal and reducing DC offset voltages, according to an embodiment of the present invention. The invention is not limited to this operational description. Rather, it will be apparent to persons skilled in the relevant art(s) from the teachings herein that other operational control flows are within the scope and spirit of the present invention. In the following discussion, the steps in FIG. 123 will be described.

In step 12302, an input signal is received, wherein the input signal comprises an RF I/Q modulated signal.

In step 12304, the input signal is frequency down-converted with a first universal frequency down-conversion module to a first down-converted signal, according to a first control signal. In an embodiment, the input signal is frequency down-converted to a non-inverted I-phase signal portion of the RF I/Q modulated signal. For instance, in an embodiment, a first phase of the in-phase signal

portion of the RF I/Q modulated signal is under-sampled. In an embodiment, the RF I/Q modulated signal may be under-sampled every 3.0 cycles of a frequency of the RF I/Q modulated signal by the first control signal. Furthermore, in embodiments, a first DC offset voltage in the first down-converted signal is reduced by a capacitor of the first universal frequency down-conversion module.

In step 12306, the input signal is frequency down-converted with a second universal frequency down-conversion module to a second down-converted signal, according to a second control signal. In an embodiment, the input signal is frequency down-converted to an inverted Q-phase signal portion of the RF I/Q modulated signal. For instance, in an embodiment, a second phase of the in-phase signal portion of the RF I/Q modulated signal is under-sampled, wherein the second phase of the in-phase signal portion is of an opposite phase to the first phase under-sampled of the in-phase signal portion. The RF I/Q modulated signal may be sampled 1.5 cycles of a frequency of the RF I/Q modulated signal after under-sampling the RF I/Q modulated signal in step 12304, for example. Furthermore, in embodiments, a second DC offset voltage in the second down-converted signal is reduced by a capacitor of the second universal frequency down-conversion module.

In step 12308, the second down-converted signal is subtracted from the first down-converted signal to form a first output signal. In embodiments, a first DC offset voltage in the first down-converted signal and a second DC offset voltage in the second down-converted signal cancel one another.

In step 12310, the input signal is frequency down-converted with a third universal frequency down-conversion module to a third down-converted signal, according to a third control signal. In an embodiment, the input signal is frequency down-converted to a non-inverted Q-phase signal portion of the RF I/Q modulated signal. For instance, in an embodiment, a third phase of the quadrature-phase signal portion of the RF I/Q modulated signal is under-sampled. The RF I/Q modulated signal may be under-sampled .75 cycles of the frequency of the RF I/Q modulated signal after under-sampling of the RF I/Q modulated signal occurs in step 12304, for example.

Furthermore, in embodiments, a third DC offset voltage in the third down-converted signal is reduced by a capacitor of the third universal frequency down-conversion module.

In step 12312, the input signal is frequency down-converted with a fourth universal frequency down-conversion module to a fourth down-converted signal, according to a fourth control signal. In an embodiment, the input signal is frequency down-converted to an inverted I-phase signal portion of the RF I/Q modulated signal. For instance, in an embodiment, a fourth phase of the quadrature-phase signal portion of the RF I/Q modulated signal is under-sampled, wherein the fourth phase of the quadrature-phase signal portion is of an opposite phase to the third phase under-sampled of the quadrature-phase signal portion. In an embodiment, the RF I/Q modulated signal may be sampled 1.5 cycles of the frequency of the RF I/Q modulated signal after under-sampling of the RF I/Q modulated signal occurs in step 12304, for example. Furthermore, in embodiments, a fourth DC offset voltage in the fourth down-converted signal is reduced by a capacitor of fourth universal frequency down-conversion module.

In step 12314, the fourth down-converted signal is subtracted from the third down-converted signal to form a second output signal. In embodiments, a third DC offset voltage in the third down-converted signal and a fourth DC offset voltage in the fourth down-converted signal cancel one another.

In step 12316, a signal is re-radiated that comprises attenuated components of first, second, third, and fourth control signal pulses, wherein the attenuated components of the first, second, third, and fourth control signal pulses form a cumulative frequency, as discussed above.

In step 12318, the first, second, third, and fourth control signal pulses are configured such that the cumulative frequency is greater than a frequency of the input signal, as discussed above.

2.2.1 Example I/Q Modulation Control Signal Generator Embodiments

FIG. 104 illustrates an exemplary block diagram for I/Q modulation control signal generator 10400, according to an embodiment of the present invention. I/Q modulation control signal

generator 10400 generates I control signal 10390, inverted I control signal 10392, Q control signal 10394, and inverted Q control signal 10396 used by I/Q modulation receiver 10300 of FIG. 103. I control signal 10390 and inverted I control signal 10392 operate to down-convert the I-phase portion of an input I/Q modulated RF signal. Q control signal 10394 and inverted Q control signal 10396 act to down-convert the Q-phase portion of the input I/Q modulated RF signal. Furthermore, I/Q modulation control signal generator 10400 has the advantage of generating control signals in a manner such that resulting collective circuit re-radiation is radiated at one or more frequencies outside of the frequency range of interest. For instance, potential circuit re-radiation is radiated at a frequency substantially greater than that of the input RF carrier signal frequency.

I/Q modulation control signal generator 10400 comprises a local oscillator 10402, a first divide-by-two module 10404, a 180 degree phase shifter 10406, a second divide-by-two module 10408, a first pulse generator 10410, a second pulse generator 10412, a third pulse generator 10414, and a fourth pulse generator 10416.

Local oscillator 10402 outputs an oscillating signal 10418. FIG. 105 shows an exemplary oscillating signal 10418.

First divide-by-two module 10404 receives oscillating signal 10418, divides oscillating signal 10418 by two, and outputs a half frequency LO signal 10420 and a half frequency inverted LO signal 10426. FIG. 105 shows an exemplary half frequency LO signal 10420. Half frequency inverted LO signal 10426 is an inverted version of half frequency LO signal 10420. First divide-by-two module 10404 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

180 degree phase shifter 10406 receives oscillating signal 10418, shifts the phase of oscillating signal 10418 by 180 degrees, and outputs phase-shifted LO signal 10422. 180 degree phase shifter 10406 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s). In alternative embodiments, other amounts of phase shift may be used.

Second divide-by two module 10408 receives phase-shifted LO signal 10422, divides phase-shifted LO signal 10422 by two, and outputs a half frequency phase-shifted LO signal 10424 and a half frequency inverted phase-shifted LO signal 10428. FIG. 105 shows an exemplary half frequency phase-shifted LO signal 10424. Half frequency inverted phase-shifted LO signal 10428 is an inverted version of half frequency phase-shifted LO signal 10424. Second divide-by-two module 10408 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

First pulse generator 10410 receives half frequency LO signal 10420, generates an output pulse whenever a rising edge is received on half frequency LO signal 10420, and outputs I control signal 10390. FIG. 105 shows an exemplary I control signal 10390.

Second pulse generator 10412 receives half frequency inverted LO signal 10426, generates an output pulse whenever a rising edge is received on half frequency inverted LO signal 10426, and outputs inverted I control signal 10392. FIG. 105 shows an exemplary inverted I control signal 10392.

Third pulse generator 10414 receives half frequency phase-shifted LO signal 10424, generates an output pulse whenever a rising edge is received on half frequency phase-shifted LO signal 10424, and outputs Q control signal 10394. FIG. 105 shows an exemplary Q control signal 10394.

Fourth pulse generator 10416 receives half frequency inverted phase-shifted LO signal 10428, generates an output pulse whenever a rising edge is received on half frequency inverted phase-shifted LO signal 10428, and outputs inverted Q control signal 10396. FIG. 105 shows an exemplary inverted Q control signal 10396.

In a preferred embodiment, control signals 10390, 10392, 10394 and 10396 output pulses having a width equal to one-half of a period of I/Q modulated RF input signal 10382. The invention, however, is not limited to these pulse widths, and control signals 10390, 10392, 10394, and 10396 may comprise pulse widths of any fraction of, or multiple and fraction of, a period of I/Q modulated RF input signal 10382.

First, second, third, and fourth pulse generators 10410, 10412, 10414, and 10416 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

As shown in FIG. 105, control signals 10390, 10392, 10394, and 10396 comprise pulses that are non-overlapping. Furthermore, in this example, pulses appear on these signals in the following order: I control signal 10390, Q control signal 10394, inverted I control signal 10392, and inverted Q control signal 10396. Potential circuit re-radiation from I/Q modulation receiver 10300 may comprise frequency components from a combination of these control signals.

For example, FIG. 106 shows an overlay of pulses from I control signal 10390, Q control signal 10394, inverted I control signal 10392, and inverted Q control signal 10396. When pulses from these control signals leak to through first, second, third, and fourth UFD modules 10302, 10306, 10310, and 10314 of to antenna 10382 (shown in FIG. 103), they may be radiated from I/Q modulation receiver 10300, with a combined waveform that appears to have a primary frequency equal to four times the frequency of any single one of control signals 10390, 10392, 10394, and 10396. FIG. 105 shows an example combined control signal 10502.

FIG. 106 also shows an example I/Q modulation RF input signal 10382 overlaid upon control signals 10390, 10392, 10394, and 10396. As shown in FIG. 106, pulses on I control signal 10390 overlay and act to down-convert a positive I-phase portion of I/Q modulation RF input signal 10382. Pulses on inverted I control signal 10392 overlay and act to down-convert a negative I-phase portion of I/Q modulation RF input signal 10382. Pulses on Q control signal 10394 overlay and act to down-convert a rising Q-phase portion of I/Q modulation RF input signal 10382. Pulses on inverted Q control signal 10396 overlay and act to down-convert a falling Q-phase portion of I/Q modulation RF input signal 10382.

As FIG. 106 further shows in this example, the frequency ratio between the combination of control signals 10390, 10392, 10394, and 10396 and I/Q modulation RF input signal 10382 is 4:3. Because the frequency of the potentially re-radiated signal, combined control signal 10502, is substantially different from that of the signal being down-converted, I/Q modulation RF input signal

10382, it does not interfere with signal down-conversion as it is out of the frequency band of interest, and hence may be filtered out. In this manner, I/Q modulation receiver 10300 reduces problems due to circuit re-radiation. As will be understood by persons skilled in the relevant art(s) from the teachings herein, frequency ratios other than 4:3 may be implemented to achieve similar reduction of problems of circuit re-radiation.

It should be understood that the above control signal generator circuit example is provided for illustrative purposes only. The invention is not limited to these embodiments. Alternative embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) for I/Q modulation control signal generator 10400 will be apparent to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the present invention.

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2.2.2 Detailed Example I/Q Modulation Receiver Embodiment with Exemplary Waveforms

FIG. 107 illustrates a more detailed example circuit implementation of I/Q modulation receiver 10300, according to an embodiment of the present invention. FIGS. 108-118 show waveforms related to an example implementation of I/Q modulation receiver 10300 of FIG. 107.

FIGS. 108 and 109 show first and second input data signals 10702 and 10704 to be I/Q modulated with a RF carrier signal frequency as the I-phase and Q-phase information signals, respectively.

FIGS. 111 and 112 show the signals of FIG. 108 and 109 after modulation with a RF carrier signal frequency, respectively, as I-modulated signal 10706 and Q-modulated signal 10708.

FIG. 110 shows an I/Q modulation RF input signal 10382 formed from I-modulated signal 10706 and Q-modulated signal 10708 of FIGS. 111 and 112, respectively.

FIG. 117 shows an overlaid view of filtered I output signal 11702 and filtered inverted I output signal 11704.

FIG. 118 shows an overlaid view of filtered Q output signal 11802 and filtered inverted Q output signal 11804.

FIGS. 113 and 114 show I baseband output signal 10384 and Q baseband output signal 10386, respectfully. A data transition 11002 is indicated in both I baseband output signal 10384 and Q baseband output signal 10386. The corresponding data transition 11002 is indicated in I-modulated signal 10706 of FIG. 111, Q-modulated signal 10708 of FIG. 112, and I/Q modulation RF input signal 10382 of FIG. 110.

FIGS. 115 and 116 show I baseband output signal 10384 and Q baseband output signal 10386 over a wider time interval.

2.2.3 Example Single Channel Receiver Embodiment

FIG. 119 illustrates an exemplary single channel receiver 11900, corresponding to either the I or Q channel of I/Q modulation receiver 10300, according to an embodiment of the present invention. Single channel receiver 11900 can down-convert an input RF signal 11906 modulated according to AM, PM, FM, and other modulation schemes. Refer to Section 2.2 above for further description on the operation of single channel receiver 11900.

3. Frequency Up-Conversion

The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

An example frequency up-conversion system 300 is illustrated in FIG. 3. The frequency up-conversion system 300 is now described.

An input signal 302 (designated as "Control Signal" in FIG. 3) is accepted by a switch module 304. For purposes of example only, assume that the input signal 302 is a FM input signal 606, an example of which is shown in FIG. 6C. FM input signal 606 may have been generated by

modulating information signal 602 onto oscillating signal 604 (FIGS. 6A and 6B). It should be understood that the invention is not limited to this embodiment. The information signal 602 can be analog, digital, or any combination thereof, and any modulation scheme can be used.

The output of switch module 304 is a harmonically rich signal 306, shown for example in FIG. 6D as a harmonically rich signal 608. The harmonically rich signal 608 has a continuous and periodic waveform.

FIG. 6E is an expanded view of two sections of harmonically rich signal 608, section 610 and section 612. The harmonically rich signal 608 may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular waveform" is used to refer to waveforms that are substantially rectangular. In a similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

Harmonically rich signal 608 is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal 608. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. 6F and FIG. 6G show separately the sinusoidal components making up the first, third, and fifth harmonics of section 610 and section 612. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal 608 is shown as a square wave, there are only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. 6H.

The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal 306 and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal 306. According to an embodiment of the invention, the input signal 606 may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

A filter 308 filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired harmonic frequency or frequencies as an output signal 310, shown for example as a filtered output signal 614 in FIG. 6I.

FIG. 4 illustrates an example universal frequency up-conversion (UFU) module 401. The UFU module 401 includes an example switch module 304, which comprises a bias signal 402, a resistor or impedance 404, a universal frequency translator (UFT) 450, and a ground 408. The UFT 450 includes a switch 406. The input signal 302 (designated as "Control Signal" in FIG. 4) controls the switch 406 in the UFT 450, and causes it to close and open. Harmonically rich signal 306 is generated at a node 405 located between the resistor or impedance 404 and the switch 406.

Also in FIG. 4, it can be seen that an example filter 308 is comprised of a capacitor 410 and an inductor 412 shunted to a ground 414. The filter is designed to filter out the undesired harmonics of harmonically rich signal 306.

The invention is not limited to the UFU embodiment shown in FIG. 4.

For example, in an alternate embodiment shown in FIG. 5, an unshaped input signal 501 is routed to a pulse shaping module 502. The pulse shaping module 502 modifies the unshaped input signal 501 to generate a (modified) input signal 302 (designated as the "Control Signal" in FIG. 5). The input signal 302 is routed to the switch module 304, which operates in the manner described above. Also, the filter 308 of FIG. 5 operates in the manner described above.

The purpose of the pulse shaping module 502 is to define the pulse width of the input signal 302. Recall that the input signal 302 controls the opening and closing of the switch 406 in switch module 304. During such operation, the pulse width of the input signal 302 establishes the pulse width of the harmonically rich signal 306. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal 306 are a function of at least the pulse width of the harmonically rich signal 306. As such, the pulse width of the input signal 302 contributes to setting the relative amplitudes of the harmonics of harmonically rich signal 306.

Further details of up-conversion as described in this section are presented in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998, incorporated herein by reference in its entirety.

3.1 Universal Transmitter with 2 UFT Modules

FIG. 71A illustrates a transmitter 7102 according to embodiments of the present invention. Transmitter 7102 includes a balanced modulator/up-converter 7104, a control signal generator 7142, an optional filter 7106, and an optional amplifier 7108. Transmitter 7102 up-converts a baseband signal 7110 to produce an output signal 7140 that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator 7104 receives the baseband signal 7110 and samples the baseband signal in a differential and balanced fashion to generate a harmonically rich signal 7138. The harmonically rich signal 7138 includes multiple harmonic images, where each image contains the baseband information in the baseband signal 7110. The optional bandpass filter 7106 may be included to select a harmonic of interest (or a subset of harmonics) in the signal 7138 for transmission. The optional amplifier 7108 may be included to amplify the selected harmonic prior to transmission. The universal transmitter is further described at a high level by the flowchart 8400 that is shown in FIG. 84. A more detailed structural and operational description of the balanced modulator follows thereafter.

Referring to flowchart 8400, in step 8402, the balanced modulator 7104 receives the baseband signal 7110.

In step 8404, the balanced modulator 7104 samples the baseband signal in a differential and balanced fashion according to a first and second control signals that are phase shifted with respect to each other. The resulting harmonically rich signal 7138 includes multiple harmonic images that repeat at harmonics of the sampling frequency, where each image contains the necessary amplitude and frequency information to reconstruct the baseband signal 7110.

In embodiments of the invention, the control signals include pulses having pulse widths (or apertures) that are established to improve energy transfer to a desired harmonic of the harmonically rich signal 7138. In further embodiments of the invention, DC offset voltages are minimized between sampling modules as indicated in step 8406, thereby minimizing carrier insertion in the harmonic images of the harmonically rich signal 7138.

In step 8408, the optional bandpass filter 7106 selects the desired harmonic of interest (or a subset of harmonics) in from the harmonically rich signal 7138 for transmission.

In step 8410, the optional amplifier 7108 amplifies the selected harmonic(s) prior to transmission.

In step 8412, the selected harmonic(s) is transmitted over a communications medium.

3.1.1 Balanced Modulator Detailed Description

Referring to the example embodiment shown in FIG. 71A, the balanced modulator 7104 includes the following components: a buffer/inverter 7112; summer amplifiers 7118, 7119; UFT modules 7124 and 7128 having controlled switches 7148 and 7150, respectively; an inductor 7126; a blocking capacitor 7136; and a DC terminal 7111. As stated above, the balanced modulator 7104 differentially samples the baseband signal 7110 to generate a harmonically rich signal 7138. More specifically, the UFT modules 7124 and 7128 sample the baseband signal in differential fashion according to control signals 7123 and 7127, respectively. A DC reference voltage 7113 is applied to terminal 7111 and is uniformly distributed to the UFT modules 7124 and 7128. The distributed DC voltage 7113 prevents any DC offset voltages from developing between the UFT modules, which can lead to carrier insertion in the harmonically rich signal 7138. The operation of the balanced modulator 7104 is discussed in greater detail with reference to flowchart 8500 (FIG. 85), as follows.

In step 8402, the buffer/inverter 7112 receives the input baseband signal 7110 and generates input signal 7114 and inverted input signal 7116. Input signal 7114 is substantially similar to signal 7110, and inverted signal 7116 is an inverted version of signal 7114. As such, the buffer/inverter

7112 converts the (single-ended) baseband signal 7110 into differential input signals 7114 and 7116 that will be sampled by the UFT modules. Buffer/inverter 7112 can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step 8504, the summer amplifier 7118 sums the DC reference voltage 7113 applied to terminal 7111 with the input signal 7114, to generate a combined signal 7120. Likewise, the summer amplifier 7119 sums the DC reference voltage 7113 with the inverted input signal 7116 to generate a combined signal 7122. Summer amplifiers 7118 and 7119 can be implemented using known op amp summer circuits, and can be designed to have a specified gain or attenuation, including unity gain, although the invention is not limited to this example. The DC reference voltage 7113 is also distributed to the outputs of both UFT modules 7124 and 7128 through the inductor 7126 as is shown.

In step 8506, the control signal generator 7142 generates control signals 7123 and 7127 that are shown by way of example in FIG. 72B and FIG. 72C, respectively. As illustrated, both control signals 7123 and 7127 have the same period T_S as a master clock signal 7145 (FIG.72A), but have a pulse width (or aperture) of T_A. In the example, control signal 7123 triggers on the rising pulse edge of the master clock signal 7145, and control signal 7127 triggers on the falling pulse edge of the master clock signal 7145. Therefore, control signals 7123 and 7127 are shifted in time by 180 degrees relative to each other. In embodiments of invention, the master clock signal 7145 (and therefore the control signals 7123 and 7127) have a frequency that is a sub-harmonic of the desired output signal 7140. The invention is not limited to the example of FIGs. 72A-72C.

In one embodiment, the control signal generator 7142 includes an oscillator 7146, pulse generators 7144a and 7144b, and an inverter 7147 as shown. In operation, the oscillator 7146 generates the master clock signal 7145, which is illustrated in FIG. 72A as a periodic square wave having pulses with a period of T_S. Other clock signals could be used including but not limited to sinusoidal waves, as will be understood by those skilled in the relevant art(s). Pulse generator 7144a receives the master clock signal 7145 and triggers on the rising pulse edge, to generate the control

signal 7123. Inverter 7147 inverts the clock signal 7145 to generate an inverted clock signal 7143. The pulse generator 7144b receives the inverted clock signal 7143 and triggers on the rising pulse edge (which is the falling edge of clock signal 7145), to generate the control signal 7127.

FIGS. 89A-E illustrate example embodiments for the pulse generator 7144. FIG. 89A illustrates a pulse generator 8902. The pulse generator 8902 generates pulses 8908 having pulse width T_A from an input signal 8904. Example input signals 8904 and pulses 8908 are depicted in FIGs 89B and 89C, respectively. The input signal 8904 can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave etc. The pulse width (or aperture) T_A of the pulses 8908 is determined by delay 8906 of the pulse generator 8902. The pulse generator 8902 also includes an optional inverter 8910, which is optionally added for polarity considerations as understood by those skilled in the arts. The example logic and implementation shown for the pulse generator 8902 is provided for illustrative purposes only, and is not limiting. The actual logic employed can take many forms. Additional examples of pulse generation logic are shown in FIGs. 89D and 89E. FIG. 89D illustrates a rising edge pulse generator 8912 that triggers on the rising edge of input signal 8904. FIG. 89E illustrates a falling edge pulse generator 8916 that triggers on the falling edge of the input signal 8904.

In step 8508, the UFT module 7124 samples the combined signal 7120 according to the control signal 7123 to generate harmonically rich signal 7130. More specifically, the switch 7148 closes during the pulse widths T_A of the control signal 7123 to sample the combined signal 7120 resulting in the harmonically rich signal 7130. FIG. 71B illustrates an exemplary frequency spectrum for the harmonically rich signal 7130 having harmonic images 7152a-n. The images 7152 repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image 7152 contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7110. As discussed further below, the relative amplitude of the frequency images is generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic 7152 can be increased (or decreased) by adjusting the pulse width T_A of the control signal 7123. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer

pulse widths of T_A shift energy into the lower frequency harmonics. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGs. 3-6. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998, and incorporated herein by reference.

In step 8510, the UFT module 7128 samples the combined signal 7122 according to the control signal 7127 to generate harmonically rich signal 7134. More specifically, the switch 7150 closes during the pulse widths T_A of the control signal 7127 to sample the combined signal 7122 resulting in the harmonically rich signal 7134. The harmonically rich signal 7134 includes multiple frequency images of baseband signal 7110 that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal 7130. However, the images in the signal 7134 are phase-shifted compared to those in signal 7130 because of the inversion of signal 7116 compared to signal 7114, and because of the relative phase shift between the control signals 7123 and 7127.

In step 8512, the node 7132 sums the harmonically rich signals 7130 and 7134 to generate harmonically rich signal 7133. FIG. 71C illustrates an exemplary frequency spectrum for the harmonically rich signal 7133 that has multiple images 7154a-n that repeat at harmonics of the sampling frequency $1/T_S$. Each image 7154 includes the necessary amplitude, frequency and phase information to reconstruct the baseband signal 7110. The capacitor 7136 operates as a DC blocking capacitor and substantially passes the harmonics in the harmonically rich signal 7133 to generate harmonically rich signal 7138 at the output of the modulator 7104.

In step 8408, the optional filter 7106 can be used to select a desired harmonic image for transmission. This is represented for example by a passband 7156 that selects the harmonic image 7154c for transmission in FIG. 71C.

An advantage of the modulator 7104 is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules 7124 and 7128. DC

offset is minimized because the reference voltage 7113 contributes a consistent DC component to the input signals 7120 and 7122 through the summing amplifiers 7118 and 7119, respectively. Furthermore, the reference voltage 7113 is also directly coupled to the outputs of the UFT modules 7124 and 7128 through the inductor 7126 and the node 7132. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal 7138. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

3.1.2 Balanced Modulator Example Signal Diagrams and Mathematical Description

In order to further describe the invention, FIGs.72D-72I illustrate various example signal diagrams (vs. time) that are representative of the invention. These signal diagrams are meant for example purposes only and are not meant to be limiting. FIG. 72D illustrates a signal 7202 that is representative of the input baseband signal 7110 (FIG. 71A). FIG. 72E illustrates a step function 7204 that is an expanded portion of the signal 7202 from time t_0 to t_1, and represents signal 7114 at the output of the buffer/inverter 7112. Similarly, FIG. 72F illustrates a signal 7206 that is an inverted version of the signal 7204, and represents the signal 7116 at the inverted output of buffer/inverter 7112. For analysis purposes, a step function is a good approximation for a portion of a single bit of data (for the baseband signal 7110) because the clock rates of the control signals 7123 and 7127 are significantly higher than the data rates of the baseband signal 7110. For example, if the data rate is in the KHz frequency range, then the clock rate will preferably be in MHZ frequency range in order to generate an output signal in the GHz frequency range.

Still referring to FIGs. 72D-I, FIG. 72G illustrates a signal 7208 that an example of the harmonically rich signal 7130 when the step function 7204 is sampled according to the control signal

7123 in FIG. 72B. The signal 7208 includes positive pulses 7209 as referenced to the DC voltage 7113. Likewise, FIG. 72H illustrates a signal 7210 that is an example of the harmonically rich signal 7134 when the step function 7206 is sampled according to the control signal 7127. The signal 7210 includes negative pulses 7211 as referenced to the DC voltage 7113, which are time-shifted relative to positive pulses 7209 in signal 7208.

Still referring to FIGs. 72D-I, the FIG. 72I illustrates a signal 7212 that is the combination of signal 7208 (FIG. 72G) and the signal 7210 (FIG. 72H), and is an example of the harmonically rich signal 7133 at the output of the summing node 7132. As illustrated, the signal 7212 spends approximately as much time above the DC reference voltage 7113 as below the DC reference voltage 7113 over a limited time period. For example, over a time period 7214, the energy in the positive pulses 7209a-b is canceled out by the energy in the negative pulses 7211a-b. This is indicative of minimal (or zero) DC offset between the UFT modules 7124 and 7128, which results in minimal carrier insertion during the sampling process.

Still referring to FIG. 72I, the time axis of the signal 7212 can be phased in such a manner to represent the waveform as an odd function. For such an arrangement, the Fourier series is readily calculated to obtain:

$$I_c(t) = \sum_{n=1}^{\infty} \left(\frac{4 \sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right) \cdot \sin\left(\frac{2n\pi t}{T_s}\right) \qquad \textit{Equation 1.}$$

where: T_S = period of the master clock 7145

T_A = pulse width of the control signals 7123 and 7127

n= harmonic number

As shown by Equation 1, the relative amplitude of the frequency images is generally a function of the harmonic number *n,* and the ratio of T_A/T_S. As indicated, the T_A/T_S ratio represents the ratio of the pulse width of the control signals relative to the period of the sub-harmonic master clock. The T_A/T_S ratio can be optimized in order to maximize the amplitude of the frequency image at a given harmonic. For example, if a passband waveform is desired to be created at 5x the frequency of the sub-harmonic clock, then a baseline power for that harmonic extraction may be calculated for the fifth harmonic (n=5) as:

$$I_c(t) = \left(\frac{4 \sin\left(\frac{5\pi T_A}{T_s} \right)}{5\pi} \right) \cdot \sin(5\omega_s t) \qquad \textit{Equation 2.}$$

As shown by Equation 2, $I_C(t)$ for the fifth harmonic is a sinusoidal function having an amplitude that is proportional to the sin $(5\pi T_A/T_S)$. The signal amplitude can be maximized by setting $T_A = (1/10 \cdot T_S)$ so that sin $(5\pi T_A/T_S) = \sin(\pi/2) = 1$. Doing so results in the equation:

$$I_c(t)\big|_{n=5} = \frac{4}{5\pi}\left(\sin\left(5\omega_s t\right)\right) \qquad \textit{Equation 3.}$$

This component is a frequency at 5x of the sampling frequency of sub-harmonic clock, and can be extracted from the Fourier series via a bandpass filter (such as bandpass filter 7106) that is centered around $5f_S$. The extracted frequency component can then be optionally amplified by the amplifier 7108 prior to transmission on a wireless or wire-line communications channel or channels.

Equation 3 can be extended to reflect the inclusion of a message signal as illustrated by equation 4 below:

$$m(t)\cdot I_c(t)\Big|_{\substack{n=5\\ \theta=\theta(t)}} = \frac{4\cdot m(t)}{5\pi}\Big(\sin\big(5\omega_s t + 5\theta(t)\big)\Big) \qquad \textit{Equation 4.}$$

Equation 4 illustrates that a message signal can be carried in harmonically rich signals 7133 such that both amplitude and phase can be modulated. In other words, m(t) is modulated for amplitude and θ(t) is modulated for phase. In such cases, it should be noted that θ(t) is augmented modulo *n* while the amplitude modulation *m(t)* is simply scaled. Therefore, complex waveforms may be reconstructed from their Fourier series with multiple aperture UFT combinations.

As discussed above, the signal amplitude for the 5th harmonic was maximized by setting the sampling aperture width T_A= 1/10 T_S, where T_S is the period of the master clock signal. This can be restated and generalized as setting T_A= ½ the period (or π radians) at the harmonic of interest. In other words, the signal amplitude of any harmonic *n* can be maximized by sampling the input waveform with a sampling aperture of T_A= ½ the period of the harmonic of interest (*n*). Based on this discussion, it is apparent that varying the aperture changes the harmonic and amplitude content of the output waveform. For example, if the sub-harmonic clock has a frequency of 200 MHZ, then the fifth harmonic is at 1Ghz. The amplitude of the fifth harmonic is maximized by setting the aperture width T_A= 500 picoseconds, which equates to ½ the period (or π radians) at 1 Ghz.

FIG. 72J depicts a frequency plot 7216 that graphically illustrates the effect of varying the sampling aperture of the control signals on the harmonically rich signal 7133 given a 200 MHZ harmonic clock. The frequency plot 7216 compares two frequency spectrums 7218 and 7220 for different control signal apertures given a 200 MHZ clock. More specifically, the frequency spectrum 7218 is an example spectrum for signal 7133 given the 200 MHZ clock with the aperture T_A = 500 psec (where 500 psec is π radians at the 5th harmonic of 1GHz). Similarly, the frequency spectrum 7220 is an example spectrum for signal 7133 given a 200 MHZ clock that is a square wave (so T_A = 5000 psec). The spectrum 7218 includes multiple harmonics 7218a-i, and the frequency spectrum

7220 includes multiple harmonics 7220a-e. [It is noted that spectrum 7220 includes only the odd harmonics as predicted by Fourier analysis for a square wave.] At 1 Ghz (which is the 5th harmonic), the signal amplitude of the two frequency spectrums 7218e and 7220c are approximately equal. However, at 200 MHZ, the frequency spectrum 7218a has a much lower amplitude than the frequency spectrum 7220a, and therefore the frequency spectrum 7218 is more efficient than the frequency spectrum 7220, assuming the desired harmonic is the 5th harmonic. In other words, assuming 1 GHz is the desired harmonic, the frequency spectrum 7218 wastes less energy at the 200 MHZ fundamental than does the frequency spectrum 7218.

3.1.3 Balanced Modulator Having a Shunt Configuration

FIG. 79A illustrates a universal transmitter 7900 that is a second embodiment of a universal transmitter having two balanced UFT modules in a shunt configuration. (In contrast, the balanced modulator 7104 can be described as having a series configuration based on the orientation of the UFT modules.) Transmitter 7900 includes a balanced modulator 7901, the control signal generator 7142, the optional bandpass filter 7106, and the optional amplifier 7108. The transmitter 7900 up-converts a baseband signal 7902 to produce an output signal 7936 that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator 7901 receives the baseband signal 7902 and shunts the baseband signal to ground in a differential and balanced fashion to generate a harmonically rich signal 7934. The harmonically rich signal 7934 includes multiple harmonic images, where each image contains the baseband information in the baseband signal 7902. In other words, each harmonic image includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7902. The optional bandpass filter 7106 may be included to select a harmonic of interest (or a subset of harmonics) in the signal 7934 for transmission. The optional amplifier 7108 may be included to amplify the selected harmonic prior to transmission, resulting in the output signal 7936.

The balanced modulator 7901 includes the following components: a buffer/inverter 7904; optional impedances 7910, 7912; UFT modules 7916 and 7922 having controlled switches 7918 and 7924, respectively; blocking capacitors 7928 and 7930; and a terminal 7920 that is tied to ground. As stated above, the balanced modulator 7901 differentially shunts the baseband signal 7902 to ground, resulting in a harmonically rich signal 7934. More specifically, the UFT modules 7916 and 7922 alternately shunts the baseband signal to terminal 7920 according to control signals 7123 and 7127, respectively. Terminal 7920 is tied to ground and prevents any DC offset voltages from developing between the UFT modules 7916 and 7922. As described above, a DC offset voltage can lead to undesired carrier insertion. The operation of the balanced modulator 7901 is described in greater detail according to the flowchart 8600 (FIG. 86) as follows.

In step 8402, the buffer/inverter 7904 receives the input baseband signal 7902 and generates I signal 7906 and inverted I signal 7908. I signal 7906 is substantially similar to the baseband signal 7902, and the inverted I signal 7908 is an inverted version of signal 7902. As such, the buffer/inverter 7904 converts the (single-ended) baseband signal 7902 into differential signals 7906 and 7908 that are sampled by the UFT modules. Buffer/inverter 7904 can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step 8604, the control signal generator 7142 generates control signals 7123 and 7127 from the master clock signal 7145. Examples of the master clock signal 7145, control signal 7123, and control signal 7127 are shown in FIGs. 72A-C, respectively. As illustrated, both control signals 7123 and 7127 have the same period T_S as a master clock signal 7145, but have a pulse width (or aperture) of T_A. Control signal 7123 triggers on the rising pulse edge of the master clock signal 7145, and control signal 7127 triggers on the falling pulse edge of the master clock signal 7145. Therefore, control signals 7123 and 7127 are shifted in time by 180 degrees relative to each other. A specific embodiment of the control signal generator 7142 is illustrated in FIG. 71A, and was discussed in detail above.

In step 8606, the UFT module 7916 shunts the signal 7906 to ground according to the control signal 7123, to generate a harmonically rich signal 7914. More specifically, the switch 7918 closes and shorts the signal 7906 to ground (at terminal 7920) during the aperture width T_A of the control signal 7123, to generate the harmonically rich signal 7914. FIG. 79B illustrates an exemplary frequency spectrum for the harmonically rich signal 7918 having harmonic images 7950a-n. The images 7950 repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image 7950 contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7902. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGs. 3-6. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998, and incorporated herein by reference.

The relative amplitude of the frequency images 7950 are generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic 7950 can be increased (or decreased) by adjusting the pulse width T_A of the control signal 7123. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics, as described by equations 1-4 above. Additionally, the relative amplitude of a particular harmonic 7950 can also be adjusted by adding/tuning an optional impedance 7910. Impedance 7910 operates as a filter that emphasizes a particular harmonic in the harmonically rich signal 7914.

In step 8608, the UFT module 7922 shunts the inverted signal 7908 to ground according to the control signal 7127, to generate a harmonically rich signal 7926. More specifically, the switch 7924 closes during the pulse widths T_A and shorts the inverted I signal 7908 to ground (at terminal 7920), to generate the harmonically rich signal 7926. At any given time, only one of input signals 7906 or 7908 is shorted to ground because the pulses in the control signals 7123 and 7127 are phase shifted with respect to each other, as shown in FIGs. 72B and 72C.

The harmonically rich signal 7926 includes multiple frequency images of baseband signal 7902 that repeat at harmonics of the sampling frequency ($1/T_S$), similar to that for the harmonically rich signal 7914. However, the images in the signal 7926 are phase-shifted compared to those in signal 7914 because of the inversion of the signal 7908 compared to the signal 7906, and because of the relative phase shift between the control signals 7123 and 7127. The optional impedance 7912 can be included to emphasis a particular harmonic of interest, and is similar to the impedance 7910 above.

In step 8610, the node 7932 sums the harmonically rich signals 7914 and 7926 to generate the harmonically rich signal 7934. The capacitors 7928 and 7930 operate as blocking capacitors that substantially pass the respective harmonically rich signals 7914 and 7926 to the node 7932. (The capacitor values may be chosen to substantially block baseband frequency components as well.) FIG. 79C illustrates an exemplary frequency spectrum for the harmonically rich signal 7934 that has multiple images 7952a-n that repeat at harmonics of the sampling frequency $1/T_S$. Each image 7952 includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 7902. The optional filter 7106 can be used to select the harmonic image of interest for transmission. This is represented by a passband 7956 that selects the harmonic image 7932c for transmission.

An advantage of the modulator 7901 is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules 7912 and 7914. DC offset is minimized because the UFT modules 7916 and 7922 are both connected to ground at terminal 7920. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal 7934. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

3.1.4 Balanced Modulator FET Configuration

As described above, the balanced modulators 7104 and 7901 utilize two balanced UFT modules to sample the input baseband signals to generate harmonically rich signals that contain the up-converted baseband information. More specifically, the UFT modules include controlled switches that sample the baseband signal in a balanced and differential fashion. FIGs. 71D and 79D illustrate embodiments of the controlled switch in the UFT module.

FIG. 71D illustrates an example transmitter 7162, according to an embodiment of the present invention. Transmitter 7162 comprises modulator 7104 (FIG. 71B) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches 7148 and 7128 are embodied as FET 7158 and FET 7160, respectively. The FET 7158 and 7160 are oriented so that their gates are controlled by the control signals 7123 and 7127, so that the control signals control the FET conductance. For the FET 7158, the combined baseband signal 7120 is received at the source of the FET 7158 and is sampled according to the control signal 7123 to produce the harmonically rich signal 7130 at the drain of the FET 7158. Likewise, the combined baseband signal 7122 is received at the source of the FET 7160 and is sampled according to the control signal 7127 to produce the harmonically rich signal 7134 at the drain of FET 7160. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs. In other words, the combined baseband signal can be received at the drain of the FETs, and the harmonically rich signals can be taken from the source of the FETs, as will be understood by those skilled in the relevant arts.

FIG. 79D illustrates an embodiment of the modulator 7900 (FIG. 79A) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches 7918 and 7924 are embodied as FET 7936 and FET 7938, respectively. The FETs 7936 and 7938 are oriented so that their gates are controlled by the control signals 7123 and 7127, respectively, so that the control signals determine FET conductance. For the FET 7936, the baseband signal 7906 is received at the source of the FET 7936 and shunted to ground according to the control signal 7123,

to produce the harmonically rich signal 7914. Likewise, the baseband signal 7908 is received at the source of the FET 7938 and is shunted to grounding according to the control signal 7127, to produce the harmonically rich signal 7926. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs, as will be understood by those skilled in the relevant arts.

3.1.5 Universal Transmitter Configured for Carrier Insertion

As discussed above, the transmitters 7102 and 7900 have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the output signal 7140. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, the present invention can be configured to provide the necessary carrier insertion by implementing a DC offset between the two sampling UFT modules.

FIG. 73A illustrates a transmitter 7302 that up-converts a baseband signal 7306 to an output signal 7322 having carrier insertion. As is shown, the transmitter 7302 is similar to the transmitter 7102 (FIG. 71A) with the exception that the up-converter/modulator 7304 is configured to accept two DC references voltages. In contrast, modulator 7104 was configured to accept only one DC reference voltage. More specifically, the modulator 7304 includes a terminal 7309 to accept a DC reference voltage 7308, and a terminal 7313 to accept a DC reference voltage 7314. Vr 7308 appears at the UFT module 7124 though summer amplifier 7118 and the inductor 7310. Vr 7314 appears at UFT module 7128 through the summer amplifier 7119 and the inductor 7316. Capacitors 7312 and 7318 operate as blocking capacitors. If Vr 7308 is different from Vr 7314 then a DC offset voltage will be exist between UFT module 7124 and UFT module 7128, which will be up-converted at the carrier frequency in the harmonically rich signal 7320. More specifically, each harmonic image in the harmonically rich signal 7320 will include a carrier signal as depicted in FIG. 73B.

FIG. 73B illustrates an exemplary frequency spectrum for the harmonically rich signal 7320 that has multiple harmonic images 7324a-n. In addition to carrying the baseband information in the sidebands, each harmonic image 7324 also includes a carrier signal 7326 that exists at respective harmonic of the sampling frequency $1/T_S$. The amplitude of the carrier signal increases with increasing DC offset voltage. Therefore, as the difference between Vr 7308 and Vr 7314 widens, the amplitude of each carrier signal 7326 increases. Likewise, as the difference between Vr 7308 and Vr 7314 shrinks, the amplitude of each carrier signal 7326 shrinks. As with transmitter 7302, the optional bandpass filter 7106 can be included to select a desired harmonic image for transmission. This is represented by passband 7328 in FIG. 73B.

3.2 Universal Transmitter In I/Q Configuration:

As described above, the balanced modulators 7104 and 7901 up-convert a baseband signal to a harmonically rich signal having multiple harmonic images of the baseband information. By combining two balanced modulators, I/Q configurations can be formed for up-converting I and Q baseband signals. In doing so, either the (series type) balanced modulator 7104 or the (shunt type) balanced modulator can be utilized. I/Q modulators having both series and shunt configurations are described below.

3.2.1 I/Q Transmitter Using Series-Type Balanced Modulator

FIG. 74 illustrates an I/Q transmitter 7420 with an in-phase (I) and quadrature (Q) configuration according to embodiments of the invention. The transmitter 7420 includes an I/Q balanced modulator 7410, an optional filter 7414, and an optional amplifier 7416. The transmitter 7420 is useful for transmitting complex I Q waveforms and does so in a balanced manner to control DC offset and carrier insertion. In doing so, the modulator 7410 receives an I baseband signal 7402 and a Q baseband signal 7404 and up-converts these signals to generate a combined harmonically

rich signal 7412. The harmonically rich signal 7412 includes multiple harmonics images, where each image contains the baseband information in the I signal 7402 and the Q signal 7404. The optional bandpass filter 7414 may be included to select a harmonic of interest (or subset of harmonics) from the signal 7412 for transmission. The optional amplifier 7416 may be included to amplify the selected harmonic prior to transmission, to generate the I/Q output signal 7418.

As stated above, the balanced I/Q modulator 7410 up-converts the I baseband signal 7402 and the Q baseband signal 7404 in a balanced manner to generate the combined harmonically rich signal 7412 that carriers the I and Q baseband information. To do so, in an embodiment, the modulator 7410 utilizes two balanced modulators 7104 from FIG. 71A, a signal combiner 7408, and a DC terminal 7407. The operation of the balanced modulator 7410 and other circuits in the transmitter is described according to the flowchart 8700 in FIG. 87, as follows. It is again noted that the ordering of steps in flowcharts is flexible, and not limited to the particular embodiments discussed herein.

In step 8702, the I/Q modulator 7410 receives the I baseband signal 7402 and the Q baseband signal 7404.

In step 8704, the I balanced modulator 7104a samples the I baseband signal 7402 in a differential fashion using the control signals 7123 and 7127 to generate a harmonically rich signal 7411a. The harmonically rich signal 7411a contains multiple harmonic images of the I baseband information, similar to the harmonically rich signal 7130 in FIG. 71B.

In step 8706, the balanced modulator 7104b samples the Q baseband signal 7404 in a differential fashion using control signals 7123 and 7127 to generate harmonically rich signal 7411b, where the harmonically rich signal 7411b contains multiple harmonic images of the Q baseband signal 7404. The operation of the balanced modulator 7104 and the generation of harmonically rich signals was fully described above and illustrated in FIGs. 71A-C, to which the reader is referred for further details.

In step 8708, the DC terminal 7407 receives a DC voltage 7406 that is distributed to both modulators 7104a and 7104b. The DC voltage 7406 is distributed to both the input and output of

both UFT modules 7124 and 7128 in each modulator 7104. This minimizes (or prevents) DC offset voltages from developing between the four UFT modules, and thereby minimizes or prevents any carrier insertion during the sampling steps 8704 and 8706.

In step 8710, the 90 degree signal combiner 7408 combines the harmonically rich signals 7411a and 7411b to generate I/Q harmonically rich signal 7412. This is further illustrated in FIGs. 75A-C. FIG. 75A depicts an exemplary frequency spectrum for the harmonically rich signal 7411a having harmonic images 7502a-n. The images 7502 repeat at harmonics of the sampling frequency $1/T_S$, where each image 7502 contains the necessary amplitude and frequency information to reconstruct the I baseband signal 7402. Likewise, FIG. 75B depicts an exemplary frequency spectrum for the harmonically rich signal 7411b having harmonic images 7504a-n. The harmonic images 7504a-n also repeat at harmonics of the sampling frequency $1/T_S$, where each image 7504 contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal 7404. FIG.75C illustrates an exemplary frequency spectrum for the combined harmonically rich signal 7412 having images 7506. Each image 7506 carries the I baseband information and the Q baseband information from the corresponding images 7502 and 7504, respectively, without substantially increasing the frequency bandwidth occupied by each harmonic 7506. This can occur because the signal combiner 7408 phase shifts the Q signal 7411b by 90 degrees relative to the I signal 7411a. The result is that the images 7502a-n and 7504a-n effectively share the signal bandwidth do to their orthogonal relationship. For example, the images 7502a and 7504a effectively share the frequency spectrum that is represented by the image 7506a.

In step 8712, the optional filter 7414 can be included to select a harmonic of interest, as represented by the passband 7508 selecting the image 7506c in FIG. 75c.

In step 8714, the optional amplifier 7416 can be included to amplify the harmonic (or harmonics) of interest prior to transmission.

In step 8716, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. 76A illustrates a transmitter 7608 that is a second embodiment for an I Q transmitter having a balanced configuration. Transmitter 7608 is similar to the transmitter 7420 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays 7604a and 7604b delay the control signals 7123 and 7127 for the Q channel modulator 7104b by 90 degrees relative the control signals for the I channel modulator 7104a. As a result, the Q modulator 7104b samples the Q baseband signal 7404 with 90 degree delay relative to the sampling of the I baseband signal 7402 by the I channel modulator 7104a. Therefore, the Q harmonically rich signal 7411b is phase shifted by 90 degrees relative to the I harmonically rich signal. Since the phase shift is achieved using the control signals, an in-phase signal combiner 7606 combines the harmonically rich signals 7411a and 7411b, to generate the harmonically rich signal 7412. It is noted that other embodiments may employ phase shifts other than 90 degrees.

FIG. 76B illustrates a transmitter 7618 that is similar to transmitter 7608 in FIG. 76A. The difference being that the transmitter 7618 has a modulator 7620 that utilizes a summing node 7622 to sum the signals 7411a and 7411b instead of the in-phase signal combiner 7606 that is used in modulator 7602 of transmitter 7608.

3.2.2. I/Q Transmitter Using Shunt-Type Balanced Modulator

FIG. 80 illustrates an I/Q transmitter 8000 that is another I/Q transmitter embodiment according to the present invention. The transmitter 8000 includes an I/Q balanced modulator 8001, an optional filter 8012, and an optional amplifier 8014. During operation, the modulator 8001 up-converts an I baseband signal 8002 and a Q baseband signal 8004 to generate a combined harmonically rich signal 8011. The harmonically rich signal 8011 includes multiple harmonics images, where each image contains the baseband information in the I signal 8002 and the Q signal 8004. The optional bandpass filter 8012 may be included to select a harmonic of interest (or subset of harmonics) from the harmonically rich signal 8011 for transmission. The optional amplifier 8014

may be included to amplify the selected harmonic prior to transmission, to generate the I/Q output signal 8016.

The I/Q modulator 8001 includes two balanced modulators 7901 from FIG. 79A, and a 90 degree signal combiner 8010 as shown. The operation of the I/Q modulator 8001 is described in reference to the flowchart 8800 (FIG. 88), as follows. The order of the steps in flowchart 8800 is not limiting.

In step 8802, the balanced modulator 8001 receives the I baseband signal 8002 and the Q baseband signal 8004.

In step 8804, the balanced modulator 7901a differentially shunts the I baseband signal 8002 to ground according the control signals 7123 and 7127, to generate a harmonically rich signal 8006. More specifically, the UFT modules 7916a and 7922a alternately shunt the I baseband signal and an inverted version of the I baseband signal to ground according to the control signals 7123 and 7127, respectively. The operation of the balanced modulator 7901 and the generation of harmonically rich signals was fully described above and is illustrated in FIGs. 79A-C, to which the reader is referred for further details. As such, the harmonically rich signal 8006 contains multiple harmonic images of the I baseband information as described above.

In step 8806, the balanced modulator 7901b differentially shunts the Q baseband signal 8004 to ground according to control signals 7123 and 7127, to generate harmonically rich signal 8008. More specifically, the UFT modules 7916b and 7922b alternately shunt the Q baseband signal and an inverted version of the Q baseband signal to ground, according to the control signals 7123 and 7127, respectively. As such, the harmonically rich signal 8008 contains multiple harmonic images that contain the Q baseband information.

In step 8808, the 90 degree signal combiner 8010 combines the harmonically rich signals 8006 and 8008 to generate I/Q harmonically rich signal 8011. This is further illustrated in FIGs. 81A-C. FIG. 81A depicts an exemplary frequency spectrum for the harmonically rich signal 8006 having harmonic images 8102a-n. The harmonic images 8102 repeat at harmonics of the sampling frequency $1/T_S$, where each image 8102 contains the necessary amplitude, frequency, and phase information

to reconstruct the I baseband signal 8002. Likewise, FIG. 81B depicts an exemplary frequency spectrum for the harmonically rich signal 8008 having harmonic images 8104a-n. The harmonic images 8104a-n also repeat at harmonics of the sampling frequency $1/T_S$, where each image 8104 contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal 8004. FIG.81C illustrates an exemplary frequency spectrum for the I/Q harmonically rich signal 8011 having images 8106a-n. Each image 8106 carries the I baseband information and the Q baseband information from the corresponding images 8102 and 8104, respectively, without substantially increasing the frequency bandwidth occupied by each image 8106. This can occur because the signal combiner 8010 phase shifts the Q signal 8008 by 90 degrees relative to the I signal 8006.

In step 8810, the optional filter 8012 may be included to select a harmonic of interest, as represented by the passband 8108 selecting the image 8106c in FIG. 81C.

In step 8812, the optional amplifier 8014 can be included to amplify the selected harmonic image 8106 prior to transmission.

In step 8814, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. 82 illustrates a transmitter 8200 that is another embodiment for an I Q transmitter having a balanced configuration. Transmitter 8200 is similar to the transmitter 8000 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays 8204a and 8204b delay the control signals 7123 and 7127 for the Q channel modulator 7901b by 90 degrees relative the control signals for the I channel modulator 7901a. As a result, the Q modulator 7901b samples the Q baseband signal 8004 with a 90 degree delay relative to the sampling of the I baseband signal 8002 by the I channel modulator 7901a. Therefore, the Q harmonically rich signal 8008 is phase shifted by 90 degrees relative to the I harmonically rich signal 8006. Since the phase shift is achieved using the control signals, an in-phase signal combiner 8206

combines the harmonically rich signals 8006 and 8008, to generate the harmonically rich signal 8011.

FIG.83 illustrates a transmitter 8300 that is similar to transmitter 8200 in FIG. 82. The difference being that the transmitter 8300 has a balanced modulator 8302 that utilizes a summing node 8304 to sum the I harmonically rich signal 8006 and the Q harmonically rich signal 8008 instead of the in-phase signal combiner 8206 that is used in the modulator 8202 of transmitter 8200. The 90 degree phase shift between the I and Q channels is implemented by delaying the Q clock signals using 90 degree delays 8204, as shown.

3.2.3 I/Q Transmitters Configured for Carrier Insertion

The transmitters 7420 (FIG. 74) and 7608 (FIG. 76A) have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the I/Q output signal 7418. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, FIG. 77 illustrates a transmitter 7702 to provide any necessary carrier insertion by implementing a DC offset between the two sets of sampling UFT modules.

Transmitter 7702 is similar to the transmitter 7420 with the exception that a modulator 7704 in transmitter 7702 is configured to accept two DC reference voltages so that the I channel modulator 7104a can be biased separately from the Q channel modulator 7104b. More specifically, modulator 7704 includes a terminal 7706 to accept a DC voltage reference 7707, and a terminal 7708 to accept a DC voltage reference 7709. Voltage 7707 biases the UFT modules 7124a and 7128a in the I channel modulator 7104a. Likewise, voltage 7709 biases the UFT modules 7124b and 7128b in the Q channel modulator 7104b. When voltage 7707 is different from voltage 7709, then a DC offset will appear between the I channel modulator 7104a and the Q channel modulator 7104b, which

results in carrier insertion in the I/Q harmonically rich signal 7412. The relative amplitude of the carrier frequency energy increases in proportion to the amount of DC offset.

FIG. 78 illustrates a transmitter 7802 that is a second embodiment of an I/Q transmitter having two DC terminals to cause DC offset, and therefore carrier insertion. Transmitter 7802 is similar to transmitter 7702 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals, similar to that done in transmitter 7608. More specifically, delays 7804a and 7804b phase shift the control signals 7123 and 7127 for the Q channel modulator 7104b relative to those of the I channel modulator 7104a. As a result, the Q modulator 7104b samples the Q baseband signal 7404 with 90 degree delay relative to the sampling of the I baseband signal 7402 by the I channel modulator 7104a. Therefore, the Q harmonically rich signal 7411b is phase shifted by 90 degrees relative to the I harmonically rich signal, which is then combined by the in-phase combiner 7806.

4. Enhanced Signal Reception

The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same.

Referring to FIG. 21, transmitter 2104 accepts a modulating baseband signal 2102 and generates (transmitted) redundant spectrums 2106a-n, which are sent over communications medium 2108. Receiver 2112 recovers a demodulated baseband signal 2114 from (received) redundant spectrums 2110a-n. Demodulated baseband signal 2114 is representative of the modulating baseband signal 2102, where the level of similarity between the modulating baseband signal 2114 and the modulating baseband signal 2102 is application dependent.

Modulating baseband signal 2102 is preferably any information signal desired for transmission and/or reception. An example modulating baseband signal 2202 is illustrated in FIG. 22A, and has an associated modulating baseband spectrum 2204 and image spectrum 2203 that are illustrated in FIG. 22B. Modulating baseband signal 2202 is illustrated as an analog signal in FIG.

22a, but could also be a digital signal, or combination thereof. Modulating baseband signal 2202 could be a voltage (or current) characterization of any number of real world occurrences, including for example and without limitation, the voltage (or current) representation for a voice signal.

Each transmitted redundant spectrum 2106a-n contains the necessary information to substantially reconstruct the modulating baseband signal 2102. In other words, each redundant spectrum 2106a-n contains the necessary amplitude, phase, and frequency information to reconstruct the modulating baseband signal 2102.

FIG. 22C illustrates example transmitted redundant spectrums 2206b-d. Transmitted redundant spectrums 2206b-d are illustrated to contain three redundant spectrums for illustration purposes only. Any number of redundant spectrums could be generated and transmitted as will be explained in following discussions.

Transmitted redundant spectrums 2206b-d are centered at f_1, with a frequency spacing f_2 between adjacent spectrums. Frequencies f_1 and f_2 are dynamically adjustable in real-time as will be shown below. FIG. 22D illustrates an alternate embodiment, where redundant spectrums 2208c,d are centered on unmodulated oscillating signal 2209 at f_1 (Hz). Oscillating signal 2209 may be suppressed if desired using, for example, phasing techniques or filtering techniques. Transmitted redundant spectrums are preferably above baseband frequencies as is represented by break 2205 in the frequency axis of FIGS. 22C and 22D.

Received redundant spectrums 2110a-n are substantially similar to transmitted redundant spectrums 2106a-n, except for the changes introduced by the communications medium 2108. Such changes can include but are not limited to signal attenuation, and signal interference. FIG. 22E illustrates example received redundant spectrums 2210b-d. Received redundant spectrums 2210b-d are substantially similar to transmitted redundant spectrums 2206b-d, except that redundant spectrum 2210c includes an undesired jamming signal spectrum 2211 in order to illustrate some advantages of the present invention. Jamming signal spectrum 2211 is a frequency spectrum associated with a jamming signal. For purposes of this invention, a "jamming signal" refers to any unwanted signal, regardless of origin, that may interfere with the proper reception and reconstruction of an intended

signal. Furthermore, the jamming signal is not limited to tones as depicted by spectrum 2211, and can have any spectral shape, as will be understood by those skilled in the art(s).

As stated above, demodulated baseband signal 2114 is extracted from one or more of received redundant spectrums 2210b-d. FIG. 22F illustrates example demodulated baseband signal 2212 that is, in this example, substantially similar to modulating baseband signal 2202 (FIG. 22A); where in practice, the degree of similarity is application dependent.

An advantage of the present invention should now be apparent. The recovery of modulating baseband signal 2202 can be accomplished by receiver 2112 in spite of the fact that high strength jamming signal(s) (e.g. jamming signal spectrum 2211) exist on the communications medium. The intended baseband signal can be recovered because multiple redundant spectrums are transmitted, where each redundant spectrum carries the necessary information to reconstruct the baseband signal. At the destination, the redundant spectrums are isolated from each other so that the baseband signal can be recovered even if one or more of the redundant spectrums are corrupted by a jamming signal.

Transmitter 2104 will now be explored in greater detail. FIG. 23A illustrates transmitter 2301, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2206b-d. Transmitter 2301 includes generator 2303, optional spectrum processing module 2304, and optional medium interface module 2320. Generator 2303 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

Transmitter 2301 operates as follows. First oscillator 2302 and second oscillator 2309 generate a first oscillating signal 2305 and second oscillating signal 2312, respectively. First stage modulator 2306 modulates first oscillating signal 2305 with modulating baseband signal 2202, resulting in modulated signal 2308. First stage modulator 2306 may implement any type of modulation including but not limited to: amplitude modulation, frequency modulation, phase modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates modulated signal 2308 with second oscillating signal 2312, resulting in multiple redundant spectrums 2206a-n shown in FIG. 23B. Second stage modulator 2310 is preferably a phase

modulator, or a frequency modulator, although other types of modulation may be implemented including but not limited to amplitude modulation. Each redundant spectrum 2206a-n contains the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal 2202.

Redundant spectrums 2206a-n are substantially centered around f_1, which is the characteristic frequency of first oscillating signal 2305. Also, each redundant spectrum 2206a-n (except for 2206c) is offset from f_1 by approximately a multiple of f_2 (Hz), where f_2 is the frequency of the second oscillating signal 2312. Thus, each redundant spectrum 2206a-n is offset from an adjacent redundant spectrum by f_2 (Hz). This allows the spacing between adjacent redundant spectrums to be adjusted (or tuned) by changing f_2 that is associated with second oscillator 2309. Adjusting the spacing between adjacent redundant spectrums allows for dynamic real-time tuning of the bandwidth occupied by redundant spectrums 2206a-n.

In one embodiment, the number of redundant spectrums 2206a-n generated by transmitter 2301 is arbitrary and may be unlimited as indicated by the "a-n" designation for redundant spectrums 2206a-n. However, a typical communications medium will have a physical and/or administrative limitations (i.e. FCC regulations) that restrict the number of redundant spectrums that can be practically transmitted over the communications medium. Also, there may be other reasons to limit the number of redundant spectrums transmitted. Therefore, preferably, the transmitter 2301 will include an optional spectrum processing module 2304 to process the redundant spectrums 2206a-n prior to transmission over communications medium 2108.

In one embodiment, spectrum processing module 2304 includes a filter with a passband 2207 (FIG. 23C) to select redundant spectrums 2206b-d for transmission. This will substantially limit the frequency bandwidth occupied by the redundant spectrums to the passband 2207. In one embodiment, spectrum processing module 2304 also up converts redundant spectrums and/or amplifies redundant spectrums prior to transmission over the communications medium 2108. Finally, medium interface module 2320 transmits redundant spectrums over the communications medium 2108. In one embodiment, communications medium 2108 is an over-the-air link and medium

interface module 2320 is an antenna. Other embodiments for communications medium 2108 and medium interface module 2320 will be understood based on the teachings contained herein.

FIG. 23D illustrates transmitter 2321, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2208c-d and unmodulated spectrum 2209. Transmitter 2321 includes generator 2311, spectrum processing module 2304, and (optional) medium interface module 2320. Generator 2311 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

As shown in FIG. 23D, many of the components in transmitter 2321 are similar to those in transmitter 2301. However, in this embodiment, modulating baseband signal 2202 modulates second oscillating signal 2312. Transmitter 2321 operates as follows. First stage modulator 2306 modulates second oscillating signal 2312 with modulating baseband signal 2202, resulting in modulated signal 2322. As described earlier, first stage modulator 2306 can effect any type of modulation including but not limited to: amplitude modulation frequency modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates first oscillating signal 2304 with modulated signal 2322, resulting in redundant spectrums 2208a-n, as shown in FIG. 23E. Second stage modulator 2310 is preferably a phase or frequency modulator, although other modulators could used including but not limited to an amplitude modulator.

Redundant spectrums 2208a-n are centered on unmodulated spectrum 2209 (at f_1 Hz), and adjacent spectrums are separated by f_2 Hz. The number of redundant spectrums 2208a-n generated by generator 2311 is arbitrary and unlimited, similar to spectrums 2206a-n discussed above. Therefore, optional spectrum processing module 2304 may also include a filter with passband 2325 to select, for example, spectrums 2208c,d for transmission over communications medium 2108. In addition, optional spectrum processing module 2304 may also include a filter (such as a bandstop filter) to attenuate unmodulated spectrum 2209. Alternatively, unmodulated spectrum 2209 may be attenuated by using phasing techniques during redundant spectrum generation. Finally, (optional) medium interface module 2320 transmits redundant spectrums 2208c,d over communications medium 2108.

Receiver 2112 will now be explored in greater detail to illustrate recovery of a demodulated baseband signal from received redundant spectrums. FIG. 24A illustrates receiver 2430, which is one embodiment of receiver 2112. Receiver 2430 includes optional medium interface module 2402, down-converter 2404, spectrum isolation module 2408, and data extraction module 2414. Spectrum isolation module 2408 includes filters 2410a-c. Data extraction module 2414 includes demodulators 2416a-c, error check modules 2420a-c, and arbitration module 2424. Receiver 2430 will be discussed in relation to the signal diagrams in FIGS. 24B-24J.

In one embodiment, optional medium interface module 2402 receives redundant spectrums 2210b-d (FIG. 22E, and FIG. 24B). Each redundant spectrum 2210b-d includes the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal used to generated the redundant spectrums. However, in the present example, spectrum 2210c also contains jamming signal 2211, which may interfere with the recovery of a baseband signal from spectrum 2210c. Down-converter 2404 down-converts received redundant spectrums 2210b-d to lower intermediate frequencies, resulting in redundant spectrums 2406a-c (FIG. 24C). Jamming signal 2211 is also down-converted to jamming signal 2407, as it is contained within redundant spectrum 2406b. Spectrum isolation module 2408 includes filters 2410a-c that isolate redundant spectrums 2406a-c from each other (FIGS. 24D-24F, respectively). Demodulators 2416a-c independently demodulate spectrums 2406a-c, resulting in demodulated baseband signals 2418a-c, respectively (FIGS. 24G-24I). Error check modules 2420a-c analyze demodulate baseband signal 2418a-c to detect any errors. In one embodiment, each error check module 2420a-c sets an error flag 2422a-c whenever an error is detected in a demodulated baseband signal. Arbitration module 2424 accepts the demodulated baseband signals and associated error flags, and selects a substantially error-free demodulated baseband signal (FIG. 24J). In one embodiment, the substantially error-free demodulated baseband signal will be substantially similar to the modulating baseband signal used to generate the received redundant spectrums, where the degree of similarity is application dependent.

Referring to FIGS. 24G-I, arbitration module 2424 will select either demodulated baseband signal 2418a or 2418c, because error check module 2420b will set the error flag 2422b that is associated with demodulated baseband signal 2418b.

The error detection schemes implemented by the error detection modules include but are not limited to: cyclic redundancy check (CRC) and parity check for digital signals, and various error detections schemes for analog signal.

Further details of enhanced signal reception as described in this section are presented in U.S. Patent No. 6,061,555 "Method and System for Ensuring Reception of a Communications Signal," filed October 21, 1998, incorporated herein by reference in its entirety.

5. *Unified Down-Conversion and Filtering*

The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

FIG. 17 is a conceptual block diagram of a UDF module 1702 according to an embodiment of the present invention. The UDF module 1702 performs at least frequency translation and frequency selectivity.

The effect achieved by the UDF module 1702 is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module 1702 effectively performs input filtering.

According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

In embodiments of the invention, input signals 1704 received by the UDF module 1702 are at radio frequencies. The UDF module 1702 effectively operates to input filter these RF input signals 1704. Specifically, in these embodiments, the UDF module 1702 effectively performs input, channel select filtering of the RF input signal 1704. Accordingly, the invention achieves high selectivity at high frequencies.

The UDF module 1702 effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

Conceptually, the UDF module 1702 includes a frequency translator 1708. The frequency translator 1708 conceptually represents that portion of the UDF module 1702 that performs frequency translation (down conversion).

The UDF module 1702 also conceptually includes an apparent input filter 1706 (also sometimes called an input filtering emulator). Conceptually, the apparent input filter 1706 represents that portion of the UDF module 1702 that performs input filtering.

In practice, the input filtering operation performed by the UDF module 1702 is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter 1706 is herein referred to as an "apparent" input filter 1706.

The UDF module 1702 of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module 1702. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module 1702 can be designed with a filter center frequency f_C on the order of 900 MHZ, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as discussed herein is not applicable.

The invention exhibits additional advantages. For example, the filtering center frequency f_C of the UDF module 1702 can be electrically adjusted, either statically or dynamically.

Also, the UDF module 1702 can be designed to amplify input signals.

Further, the UDF module 1702 can be implemented without large resistors, capacitors, or inductors. Also, the UDF module 1702 does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module 1702 is friendly to integrated circuit design techniques and processes.

The features and advantages exhibited by the UDF module 1702 are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF module 1702 performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to frequency translation also contribute to the performance of frequency selectivity, and vice versa.

According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and samples/instances of the output signal.

More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

Next, the input sample is held (that is, delayed).

Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module preferably performs input filtering and frequency down-conversion in a unified manner.

FIG. 19 illustrates an example implementation of the unified down-converting and filtering (UDF) module 1922. The UDF module 1922 performs the frequency translation operation and the frequency selectivity operation in an integrated, unified manner as described above, and as further described below.

In the example of FIG. 19, the frequency selectivity operation performed by the UDF module 1922 comprises a band-pass filtering operation according to EQ. 1, below, which is an example representation of a band-pass filtering transfer function.

$$VO = \alpha_1 z^{-1} VI - \beta_1 z^{-1} VO - \beta_0 z^{-2} VO \qquad \text{EQ. 1}$$

It should be noted, however, that the invention is not limited to band-pass filtering. Instead, the invention effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof. As will be appreciated, there are many representations of any given filter type. The invention is applicable to these filter representations. Thus, EQ. 1 is referred to herein for illustrative purposes only, and is not limiting.

The UDF module 1922 includes a down-convert and delay module 1924, first and second delay modules 1928 and 1930, first and second scaling modules 1932 and 1934, an output sample and hold module 1936, and an (optional) output smoothing module 1938. Other embodiments of the UDF module will have these components in different configurations, and/or a subset of these components, and/or additional components. For example, and without limitation, in the configuration shown in FIG. 19, the output smoothing module 1938 is optional.

As further described below, in the example of FIG. 19, the down-convert and delay module 1924 and the first and second delay modules 1928 and 1930 include switches that are controlled by a clock having two phases, ϕ_1 and ϕ_2. ϕ_1 and ϕ_2 preferably have the same frequency, and are non-overlapping (alternatively, a plurality such as two clock signals having these characteristics could be used). As used herein, the term "non-overlapping" is defined as two or more signals where only one of the signals is active at any given time. In some embodiments, signals are "active" when they are high. In other embodiments, signals are active when they are low.

Preferably, each of these switches closes on a rising edge of ϕ_1 or ϕ_2, and opens on the next corresponding falling edge of ϕ_1 or ϕ_2. However, the invention is not limited to this example. As will be apparent to persons skilled in the relevant art(s), other clock conventions can be used to control the switches.

In the example of FIG. 19, it is assumed that α_1 is equal to one. Thus, the output of the down-convert and delay module 1924 is not scaled. As evident from the embodiments described above, however, the invention is not limited to this example.

The example UDF module 1922 has a filter center frequency of 900.2 MHZ and a filter bandwidth of 570 KHz. The pass band of the UDF module 1922 is on the order of 899.915 MHZ to 900.485 MHZ. The Q factor of the UDF module 1922 is approximately 1879 (i.e., 900.2 MHZ divided by 570 KHz).

The operation of the UDF module 1922 shall now be described with reference to a Table 1802 (FIG. 18) that indicates example values at nodes in the UDF module 1922 at a number of consecutive time increments. It is assumed in Table 1802 that the UDF module 1922 begins operating at time t-1. As indicated below, the UDF module 1922 reaches steady state a few time units after operation begins. The number of time units necessary for a given UDF module to reach steady state depends on the configuration of the UDF module, and will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

At the rising edge of ϕ_1 at time t-1, a switch 1950 in the down-convert and delay module 1924 closes. This allows a capacitor 1952 to charge to the current value of an input signal, VI_{t-1}, such that node 1902 is at VI_{t-1}. This is indicated by cell 1804 in FIG. 18. In effect, the combination of the switch 1950 and the capacitor 1952 in the down-convert and delay module 1924 operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Thus, the value stored in the capacitor 1952 represents an instance of a down-converted image of the input signal VI.

The manner in which the down-convert and delay module 1924 performs frequency down-conversion is further described elsewhere in this application, and is additionally described in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998, which is herein incorporated by reference in its entirety.

Also at the rising edge of ϕ_1 at time t-1, a switch 1958 in the first delay module 1928 closes, allowing a capacitor 1960 to charge to VO_{t-1}, such that node 1906 is at VO_{t-1}. This is indicated by cell 1806 in Table 1802. (In practice, VO_{t-1} is undefined at this point. However, for ease of understanding, VO_{t-1} shall continue to be used for purposes of explanation.)

Also at the rising edge of ϕ_1 at time t-1, a switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to a value stored in a capacitor 1964. At this time, however, the value in capacitor 1964 is undefined, so the value in capacitor 1968 is undefined. This is indicated by cell 1807 in table 1802.

At the rising edge of ϕ_2 at time t-1, a switch 1954 in the down-convert and delay module 1924 closes, allowing a capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_{t-1}, such that node 1904 is at VI_{t-1}. This is indicated by cell 1810 in Table 1802.

The UDF module 1922 may optionally include a unity gain module 1990A between capacitors 1952 and 1956. The unity gain module 1990A operates as a current source to enable capacitor 1956 to charge without draining the charge from capacitor 1952. For a similar reason, the UDF module 1922 may include other unity gain modules 1990B-1990G. It should be understood that, for many embodiments and applications of the invention, these unity gain modules 1990A-1990G are optional. The structure and operation of the unity gain modules 1990 will be apparent to persons skilled in the relevant art(s).

Also at the rising edge of ϕ_2 at time t-1, a switch 1962 in the first delay module 1928 closes, allowing a capacitor 1964 to charge to the level of the capacitor 1960. Accordingly, the capacitor 1964 charges to VO_{t-1}, such that node 1908 is at VO_{t-1}. This is indicated by cell 1814 in Table 1802.

Also at the rising edge of ϕ_2 at time t-1, a switch 1970 in the second delay module 1930 closes, allowing a capacitor 1972 to charge to a value stored in a capacitor 1968. At this time, however, the value in capacitor 1968 is undefined, so the value in capacitor 1972 is undefined. This is indicated by cell 1815 in table 1802.

At time t, at the rising edge of ϕ_1, the switch 1950 in the down-convert and delay module 1924 closes. This allows the capacitor 1952 to charge to VI_t, such that node 1902 is at VI_t. This is indicated in cell 1816 of Table 1802.

Also at the rising edge of ϕ_1 at time t, the switch 1958 in the first delay module 1928 closes, thereby allowing the capacitor 1960 to charge to VO_t. Accordingly, node 1906 is at VO_t. This is indicated in cell 1820 in Table 1802.

Further at the rising edge of ϕ_1 at time t, the switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to the level of the capacitor 1964. Therefore, the capacitor 1968 charges to VO_{t-1}, such that node 1910 is at VO_{t-1}. This is indicated by cell 1824 in Table 1802.

At the rising edge of ϕ_2 at time t, the switch 1954 in the down-convert and delay module 1924 closes, allowing the capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_t, such that node 1904 is at VI_t. This is indicated by cell 1828 in Table 1802.

Also at the rising edge of ϕ_2 at time t, the switch 1962 in the first delay module 1928 closes, allowing the capacitor 1964 to charge to the level in the capacitor 1960. Therefore, the capacitor 1964 charges to VO_t, such that node 1908 is at VO_t. This is indicated by cell 1832 in Table 1802.

Further at the rising edge of ϕ_2 at time t, the switch 1970 in the second delay module 1930 closes, allowing the capacitor 1972 in the second delay module 1930 to charge to the level of the capacitor 1968 in the second delay module 1930. Therefore, the capacitor 1972 charges to VO_{t-1}, such that node 1912 is at VO_{t-1}. This is indicated in cell 1836 of FIG. 18.

At time t+1, at the rising edge of ϕ_1, the switch 1950 in the down-convert and delay module 1924 closes, allowing the capacitor 1952 to charge to VI_{t+1}. Therefore, node 1902 is at VI_{t+1}, as indicated by cell 1838 of Table 1802.

Also at the rising edge of ϕ_1 at time t+1, the switch 1958 in the first delay module 1928 closes, allowing the capacitor 1960 to charge to VO_{t+1}. Accordingly, node 1906 is at VO_{t+1}, as indicated by cell 1842 in Table 1802.

Further at the rising edge of ϕ_1 at time t+1, the switch 1966 in the second delay module 1930 closes, allowing the capacitor 1968 to charge to the level of the capacitor 1964. Accordingly, the capacitor 1968 charges to VO_t, as indicated by cell 1846 of Table 1802.

In the example of FIG. 19, the first scaling module 1932 scales the value at node 1908 (i.e., the output of the first delay module 1928) by a scaling factor of -0.1. Accordingly, the value present at node 1914 at time t+1 is $-0.1 * VO_t$. Similarly, the second scaling module 1934 scales the value present at node 1912 (i.e., the output of the second scaling module 1930) by a scaling factor of -0.8. Accordingly, the value present at node 1916 is $-0.8 * VO_{t-1}$ at time t+1.

At time t+1, the values at the inputs of the summer 1926 are: VI_t at node 1904, $-0.1 * VO_t$ at node 1914, and $-0.8 * VO_{t-1}$ at node 1916 (in the example of FIG. 19, the values at nodes 1914 and 1916 are summed by a second summer 1925, and this sum is presented to the summer 1926). Accordingly, at time t+1, the summer generates a signal equal to $VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$.

At the rising edge of ϕ_1 at time t+1, a switch 1991 in the output sample and hold module 1936 closes, thereby allowing a capacitor 1992 to charge to VO_{t+1}. Accordingly, the capacitor 1992 charges to VO_{t+1}, which is equal to the sum generated by the adder 1926. As just noted, this value is equal to: $VI_t - 0.1 * VO_t - 0.8 * VO_{t-1}$. This is indicated in cell 1850 of Table 1802. This value is presented to the optional output smoothing module 1938, which smooths the signal to thereby generate the instance of the output signal VO_{t+1}. It is apparent from inspection that this value of VO_{t+1} is consistent with the band pass filter transfer function of EQ. 1.

Further details of unified down-conversion and filtering as described in this section are presented in U.S. Patent No. 6,049,706 "Integrated Frequency Translation And Selectivity," filed October 21, 1998, incorporated herein by reference in its entirety.

6. *Example Application Embodiments of the Invention*

As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

Example applications of the UFT module were described above. In particular, frequency down-conversion, frequency up-conversion, enhanced signal reception, and unified down-conversion

and filtering applications of the UFT module were summarized above, and are further described below. These applications of the UFT module are discussed herein for illustrative purposes. The invention is not limited to these example applications. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s), based on the teachings contained herein.

For example, the present invention can be used in applications that involve frequency down-conversion. This is shown in FIG. 1C, for example, where an example UFT module 115 is used in a down-conversion module 114. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal. This is also shown in FIG. 7, for example, where an example UFT module 706 is part of a down-conversion module 704, which is part of a receiver 702.

The present invention can be used in applications that involve frequency up-conversion. This is shown in FIG. 1D, for example, where an example UFT module 117 is used in a frequency up-conversion module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal. This is also shown in FIG. 8, for example, where an example UFT module 806 is part of up-conversion module 804, which is part of a transmitter 802.

The present invention can be used in environments having one or more transmitters 902 and one or more receivers 906, as illustrated in FIG. 9. In such environments, one or more of the transmitters 902 may be implemented using a UFT module, as shown for example in FIG. 8. Also, one or more of the receivers 906 may be implemented using a UFT module, as shown for example in FIG. 7.

The invention can be used to implement a transceiver. An example transceiver 1002 is illustrated in FIG. 10. The transceiver 1002 includes a transmitter 1004 and a receiver 1008. Either the transmitter 1004 or the receiver 1008 can be implemented using a UFT module. Alternatively, the transmitter 1004 can be implemented using a UFT module 1006, and the receiver 1008 can be implemented using a UFT module 1010. This embodiment is shown in FIG. 10.

Another transceiver embodiment according to the invention is shown in FIG. 11. In this transceiver 1102, the transmitter 1104 and the receiver 1108 are implemented using a single UFT module 1106. In other words, the transmitter 1104 and the receiver 1108 share a UFT module 1106.

As described elsewhere in this application, the invention is directed to methods and systems for enhanced signal reception (ESR). Various ESR embodiments include an ESR module (transmit) in a transmitter 1202, and an ESR module (receive) in a receiver 1210. An example ESR embodiment configured in this manner is illustrated in FIG. 12.

The ESR module (transmit) 1204 includes a frequency up-conversion module 1206. Some embodiments of this frequency up-conversion module 1206 may be implemented using a UFT module, such as that shown in FIG. 1D.

The ESR module (receive) 1212 includes a frequency down-conversion module 1214. Some embodiments of this frequency down-conversion module 1214 may be implemented using a UFT module, such as that shown in FIG. 1C.

As described elsewhere in this application, the invention is directed to methods and systems for unified down-conversion and filtering (UDF). An example unified down-conversion and filtering module 1302 is illustrated in FIG. 13. The unified down-conversion and filtering module 1302 includes a frequency down-conversion module 1304 and a filtering module 1306. According to the invention, the frequency down-conversion module 1304 and the filtering module 1306 are implemented using a UFT module 1308, as indicated in FIG. 13.

Unified down-conversion and filtering according to the invention is useful in applications involving filtering and/or frequency down-conversion. This is depicted, for example, in FIGS. 15A-15F. FIGS. 15A-15C indicate that unified down-conversion and filtering according to the invention is useful in applications where filtering precedes, follows, or both precedes and follows frequency down-conversion. FIG. 15D indicates that a unified down-conversion and filtering module 1524 according to the invention can be utilized as a filter 1522 (i.e., where the extent of frequency down-conversion by the down-converter in the unified down-conversion and filtering module 1524 is minimized). FIG. 15E indicates that a unified down-conversion and filtering module 1528 according to the invention can be utilized as a down-converter 1526 (i.e., where the filter in the unified down-conversion and filtering module 1528 passes substantially all frequencies). FIG. 15F illustrates that the unified down-conversion and filtering module 1532 can be used as an amplifier. It is noted that

one or more UDF modules can be used in applications that involve at least one or more of filtering, frequency translation, and amplification.

For example, receivers, which typically perform filtering, down-conversion, and filtering operations, can be implemented using one or more unified down-conversion and filtering modules. This is illustrated, for example, in FIG. 14.

The methods and systems of unified down-conversion and filtering of the invention have many other applications. For example, as discussed herein, the enhanced signal reception (ESR) module (receive) operates to down-convert a signal containing a plurality of spectrums. The ESR module (receive) also operates to isolate the spectrums in the down-converted signal, where such isolation is implemented via filtering in some embodiments. According to embodiments of the invention, the ESR module (receive) is implemented using one or more unified down-conversion and filtering (UDF) modules. This is illustrated, for example, in FIG. 16. In the example of FIG. 16, one or more of the UDF modules 1610, 1612, 1614 operates to down-convert a received signal. The UDF modules 1610, 1612, 1614 also operate to filter the down-converted signal so as to isolate the spectrum(s) contained therein. As noted above, the UDF modules 1610, 1612, 1614 are implemented using the universal frequency translation (UFT) modules of the invention.

The invention is not limited to the applications of the UFT module described above. For example, and without limitation, subsets of the applications (methods and/or structures) described herein (and others that would be apparent to persons skilled in the relevant art(s) based on the herein teachings) can be associated to form useful combinations.

For example, transmitters and receivers are two applications of the UFT module. FIG. 10 illustrates a transceiver 1002 that is formed by combining these two applications of the UFT module, i.e., by combining a transmitter 1004 with a receiver 1008.

Also, ESR (enhanced signal reception) and unified down-conversion and filtering are two other applications of the UFT module. FIG. 16 illustrates an example where ESR and unified down-conversion and filtering are combined to form a modified enhanced signal reception system.

The invention is not limited to the example applications of the UFT module discussed herein. Also, the invention is not limited to the example combinations of applications of the UFT module discussed herein. These examples were provided for illustrative purposes only, and are not limiting. Other applications and combinations of such applications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion; (4) receiving; (5) transmitting; (6) filtering; and/or (7) signal transmission and reception in environments containing potentially jamming signals.

Additional example applications are described below.

6.1 Data Communication

The invention is directed to data communication among data processing devices. For example, and without limitation, the invention is directed to computer networks such as, for example, local area networks (LANs), wide area networks (WANs), including wireless LANs (WLANs) and wireless WANs, modulator/demodulators (modems), including wireless modems, short range networks, such as Bluetooth, etc., and combinations thereof.

FIG. 25 illustrates an example environment 2502 wherein computers 2504, 2512, and 2526 communicate with one another via a computer network 2534. In the example of FIG. 25, computer 2504 is communicating with the network 2534 via a wired link, whereas computers 2512 and 2526 are communicating with the network 2534 via wireless links.

In the teachings contained herein, for illustrative purposes, a link may be designated as being a wired link or a wireless link. Such designations are for example purposes only, and are not limiting. A link designated as being wireless may alternatively be wired. Similarly, a link designated as being wired may alternatively be wireless. This is applicable throughout the entire application.

The computers 2504, 2512 and 2526 each include an interface 2506, 2514, and 2528, respectively, for communicating with the network 2534. The interfaces 2506, 2514, and 2528 include transmitters 2508, 2516, and 2530 respectively. Also, the interfaces 2506, 2514 and 2528 include receivers 2510, 2518, and 2532 respectively. In embodiments of the invention, the transmitters 2508, 2516 and 2530 are implemented using UFT modules for performing frequency up-conversion operations (see, for example, FIG. 8). In embodiments, the receivers 2510, 2518 and 2532 are implemented using UFT modules for performing frequency down-conversion operations (see, for example, FIG. 7).

As noted above, the computers 2512 and 2526 interact with the network 2534 via wireless links. In embodiments of the invention, the interfaces 2514, 2528 in computers 2512, 2526 represent modulator/demodulators (modems).

In embodiments, the network 2534 includes an interface or modem 2520 for communicating with the modems 2514, 2528 in the computers 2512, 2526. In embodiments, the interface 2520 includes a transmitter 2522, and a receiver 2524. Either or both of the transmitter 2522, and the receiver 2524 are implemented using UFT modules for performing frequency translation operations (see, for example, FIGS. 7 and 8).

In alternative embodiments, one or more of the interfaces 2506, 2514, 2520, and 2528 are implemented using transceivers that employ one or more UFT modules for performing frequency translation operations (see, for example, FIGS. 10 and 11).

FIG. 26 illustrates another example data communication embodiment 2602. Each of a plurality of computers 2604, 2612, 2614 and 2616 includes an interface, such as an interface 2606 shown in the computer 2604. It should be understood that the other computers 2612, 2614, 2616 also include an interface such as an interface 2606. The computers 2604, 2612, 2614 and 2616 communicate with each other via interfaces 2606 and wireless or wired links, thereby collectively representing a data communication network.

The interfaces 2606 may represent any computer interface or port, such as but not limited to a high speed internal interface, a wireless serial port, a wireless PS2 port, a wireless USB port, PCMCIA port, etc.

The interface 2606 includes a transmitter 2608 and a receiver 2610. In embodiments of the invention, either or both of the transmitter 2608 and the receiver 2610 are implemented using UFT modules for frequency up-conversion and down-conversion (see, for example, FIGS. 7 and 8). Alternatively, the interfaces 2806 can be implemented using a transceiver having one or more UFT modules for performing frequency translation operations (see, for example, FIGS. 10 and 11).

FIGS. 33-38 illustrate other scenarios envisioned and encompassed by the invention. FIG. 33 illustrates a data processing environment 3302 wherein a wired network, such as an Ethernet network 3304, is linked to another network, such as a WLAN 3306, via a wireless link 3308. The wireless link 3308 is established via interfaces 3310, 3312 which are preferably implemented using universal frequency translation modules.

The invention includes multiple networks linked together. The invention also envisions wireless networks conforming to any known or custom standard or specification. This is shown in FIG. 34, for example, where any combination of WLANs conforming to any WLAN standard or configuration, such as IEEE 802.11 (described in further detail elsewhere herein), any cellular telephone standard or specification, any WAN standard, any short range wireless standard, any type of radio links, any custom standard or specification, etc., can be implemented using the universal frequency translation technology described herein. Also, any combination of these networks may be coupled together. It is noted that the invention is not limited to the embodiment shown in FIG. 34.

The invention supports WLANs and/or other communication networks (and combinations thereof) that are located in one or multiple buildings, as shown in FIGS. 35 and 36. The invention also supports WLANs and/or other communication networks (and combinations thereof) that are located in an area including and external to one or more buildings, as shown in FIG. 37. In fact, the invention is directed to networks that cover any defined geographical area, as shown in FIG. 38. In

the embodiments described above, wireless links are preferably established using interfaces as described herein.

6.1.1. Example Implementations: Interfaces, Wireless Modems, Wireless LANs, etc.

The present invention is now described as implemented in an interface, such as but not limited to a wireless modem, which can be utilized to implement a wireless local area network (WLAN) or wireless wide area network (WWAN), for example. In an embodiment, the present invention is implemented in a WLAN to support IEEE WLAN Standard 802.11, but this embodiment is mentioned for illustrative purposes only. The invention is not limited to this standard or the WLAN embodiment and described herein.

Conventional wireless modems are described in, for example, U.S. Patent 5,764,693, titled, "Wireless Radio Modem with Minimal Inter-Device RF Interference," incorporated herein by reference in its entirety. The present invention replaces a substantial portion of conventional wireless modems with one or more universal frequency translators (UFTs). The resultant improved wireless modem consumes less power than conventional wireless modems and is easier and less expensive to design and build. A wireless modem in accordance with the present invention can be implemented in a PC-MCIA card or within a main housing of a computer, or on one or more chips, in any data processing or communication device (desk top, handheld, etc.) for example. The invention is not limited to these examples.

FIG. 27 illustrates an example block diagram of a device 2710, which can be wirelessly coupled to a LAN, as illustrated for example in FIGS. 25 and 26. The device 2710 includes an interface 2714 and an antenna 2712. The interface 2714 includes a transmitter module 2716 that receives information from a digital signal processor (DSP) 2720, and modulates and up-converts the information for transmission from the antenna 2712. The interface 2714 also includes a receiver module 2718 that receives modulated carrier signals via the antenna 2712. The receiver module

2718 down-converts and demodulates the modulated carrier signals to baseband information, and provides the baseband information to the DSP 2720. The DSP 2720 can include a central processing unit (CPU) and other components of the device 2710. Conventionally, the interface 2714 is implemented with heterodyne components. The device can be any data processing or communication device, or other device where communication with external devices is desired.

FIG. 28 illustrates an example interface 2810 implemented with heterodyne components. The interface 2810 includes a transmitter module 2812 and a receiver module 2824. The receiver module 2824 includes an RF section 2830, one or more IF sections 2828, a demodulator section 2826, an optional analog to digital (A/D) converter 2834, and a frequency generator/synthesizer 2832. The transmitter module 2812 includes an optional digital to analog (D/A) converter 2822, a modulator section 2818, one or more IF sections 2816, an RF section 2814, and a frequency generator/synthesizer 2820. Operation of the interface 2810 will be apparent to one skilled in the relevant art(s), based on the description herein.

FIG. 29 illustrates an example in-phase/quadrature-phase (I/Q) interface 2910 implemented with heterodyne components. I/Q implementations allow two channels of information to be communicated on a carrier signal and thus can be utilized to increase data transmission.

The interface 2910 includes a transmitter module 2912 and a receiver module 2934. The receiver module 2934 includes an RF section 2936, one or more IF sections 2938, an I/Q demodulator section 2940, an optional A/D converter 2944, and a frequency generator/synthesizer 2942. The I/Q demodulator section 2940 includes a signal splitter 2946, mixers 2948, and a phase shifter 2950. The signal splitter 2946 provides a received signal to the mixers 2948. The phase shifter 2950 operates the mixers 2948 ninety degrees out of phase with one another to generate I and Q information channels 2952 and 2954, respectively, which are provided to a DSP 2956 through the optional A/D converter 2944.

The transmitter module 2912 includes an optional D/A converter 2922, an I/Q modulator section 2918, one or more IF sections 2916, an RF section 2914, and a frequency generator/synthesizer 2920. The I/Q modulator section 2918 includes mixers 2924, a phase shifter

2926, and a signal combiner 2928. The phase shifter 2926 operates the mixers 2924 ninety degrees out of phase with one another to generate I and Q modulated information signals 2930 and 2932, respectively, which are combined by the signal combiner 2928. The IF section(s) 2916 and RF section 2914 up-convert the combined I and Q modulated information signals 2930 and 2932 to RF for transmission by the antenna, in a manner well known in the relevant art(s).

Heterodyne implementations, such as those illustrated in FIGS. 28 and 29, are expensive and difficult to design, manufacture and tune. In accordance with the present invention, therefore, the interface 2714 (FIG. 27) is preferably implemented with one or more universal frequency translation (UFT) modules, such as the UFT module 102 (FIG. 1A or other embodiments described herein, or equivalents thereof). Thus previously described benefits of the present invention are obtained in wireless modems, WLANs, or even wired devices, etc.

FIG. 30 illustrates an example block diagram embodiment of the interface 2714 that is associated with a computer or any other data processing or communication device. In FIG. 30, the receiver module 2718 includes a universal frequency down-converter (UFD) module 3014 and an optional analog to digital (A/D) converter 3016, which converts an analog output from the UFD 3014 to a digital format for the DSP 2720. The transmitter module 2716 includes an optional modulator 3012 and a universal frequency up-converter (UFU) module 3010. The optional modulator 3012 can be a variety of types of modulators, including conventional modulators. Alternatively, the UFU module 3010 includes modulator functionality. The example implementation of FIG. 30 operates substantially as described above and in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998, and U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998.

FIG. 31 illustrates an example implementation of the interface 2714 illustrated in FIG. 30, wherein the receiver UFD 3014 includes a UFT module 3112, and the transmitter UFU 3010 includes a universal frequency translation (UFT) module 3110. This example implementation operates substantially as described above and in U.S. Patent No. 6,061,551 entitled "Method and

System for Down-Converting Electromagnetic Signals," filed October 21, 1998, and U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998.

FIG. 32 illustrates an example I/Q implementation of the interface module 2710. Other I/Q implementations are also contemplated and are within the scope of the present invention.

In the example of FIG. 32, the receiver UFD module 3014 includes a signal divider 3228 that provides a received I/Q modulated carrier signal 3230 between a third UFT module 3224 and a fourth UFT module 3226. A phase shifter 3232, illustrated here as a 90 degree phase shifter, controls the third and fourth UFT modules 3224 and 3226 to operate 90 degrees out of phase with one another. As a result, the third and fourth UFT modules 3224 and 3226 down-convert and demodulate the received I/Q modulated carrier signal 3230, and output I and Q channels 3234 and 3236, respectively, which are provided to the DSP 2720 through the optional A/D converter 3016.

In the example of FIG. 32, the transmitter UFU module 3010 includes first and second UFT modules 3212 and 3214 and a phase shifter 3210, which is illustrated here as a 90 degree phase shifter. The phase shifter 3210 receives a lower frequency modulated carrier signal 3238 from the modulator 3012. The phase shifter 3210 controls the first and second UFT modules 3212 and 3214 to operate 90 degrees out of phase with one another. The first and second UFT modules 3212 and 3214 up-convert the lower frequency modulated carrier signal 3238, which are output as higher frequency modulated I and Q carrier channels 3218 and 3220, respectively. A signal combiner 3216 combines the higher frequency modulated I and Q carrier channels 3218 and 3220 into a single higher frequency modulated I/Q carrier signal 3222 for transmitting by the antenna 2712.

The example implementations of the interfaces described above, and variations thereof, can also be used to implement network interfaces, such as the network interface 2520 illustrated in FIG. 25.

More generally, the invention is directed to WLAN client devices and WLAN infrastructure devices. "WLAN Client Devices" refers to, for example, any data processing and/or communication devices in which wired or wireless communication functionality is desired, such as but not limited to computers, personal data assistants (PDAs), automatic identification data collection devices (such

as bar code scanners/readers, electronic article surveillance readers, and radio frequency identification readers), telephones, network devices, etc., and combinations thereof. "WLAN Infrastructure Devices" refers to, for example, Access Points and other devices used to provide the ability for WLAN Client Devices (as well as potentially other devices) to connect to wired and/or wireless networks and/or to provide the network functionality of a WLAN. "WLAN" refers to, for example, a Wireless Local Area Network that is implemented according to and that operates within WLAN standards and/or specifications, such as but not limited to IEEE 802.11, IEEE 802.11a, IEEE 802.11b, HomeRF, Proxim Range LAN, Proxim Range LAN2, Symbol Spectrum 1, Symbol Spectrum 24 as it existed prior to adoption of IEEE 802.11, HiperLAN1, or HiperLAN2. WLAN client devices and/or WLAN infrastructure devices may operate in a multi-mode capacity. For example, a device may include WLAN and WAN functionality. Another device may include WLAN and short range communication (such as but not limited to Blue Tooth) functionality. Another device may include WLAN and WAN and short range communication functionality. It is noted that the above definitions and examples are provided for illustrative purposes, and are not limiting. Equivalents to that described above will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.1.2 Example Modifications

The RF modem applications, WLAN applications, etc., described herein, can be modified by incorporating one or more of the enhanced signal reception (ESR) techniques described herein. Use of ESR embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The RF modem applications, WLAN applications, etc., described herein can be enhanced by incorporating one or more of the unified down-conversion and filtering (UDF) techniques described herein. Use of UDF embodiments with the network embodiments described herein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.2. Other Example Applications

The application embodiments described above are provided for purposes of illustration. These applications and embodiments are not intended to limit the invention. Alternate and additional applications and embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, such alternate and additional applications and embodiments include combinations of those described above. Such combinations will be apparent to persons skilled in the relevant art(s) based on the herein teachings.

6.3. Example WLAN Implementation Embodiments

6.3.1. Architecture

FIG. 39 is a block diagram of a WLAN interface 3902 (also referred to as a WLAN modem herein) according to an embodiment of the invention. The WLAN interface/modem 3902 includes an antenna 3904, a low noise amplifier or power amplifier (LNA/PA) 3904, a receiver 3906, a transmitter 3910, a control signal generator 3908, a demodulator/modulator facilitation module 3912, and a media access controller (MAC) interface 3914. The MAC interface 3914 couples the WLAN interface/modem 3902 to a computer 3916 or other data processing or communication device. The computer 3916 preferably includes a MAC 3918.

The WLAN interface/modem 3902 represents a transmit and receive application that utilizes the universal frequency translation technology described herein. It also represents a zero IF (or direct-to-data) WLAN architecture.

The WLAN interface/modem 3902 also represents a vector modulator and a vector demodulator using the universal frequency translation (UFT) technology described herein. Use of the UFT technology enhances the flexibility of the WLAN application (i.e., makes it universal).

In the embodiment shown in FIG. 39, the WLAN interface/modem 3902 is compliant with WLAN standard IEEE 802.11. However, the invention is not limited to this standard. The invention is applicable to any communication standard or specification, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein. Any modifications to the invention to operate with other standards or specifications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. 39, the WLAN interface/modem 3902 provides half duplex communication. However, the invention is not limited to this communication mode. The invention is applicable and directed to other communication modes, as will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

In the embodiment shown in FIG. 39, the modulation/demodulation performed by the WLAN interface/modem 3902 is preferably direct sequence spread spectrum QPSK (quadrature phase shift keying) with differential encoding. However, the invention is not limited to this modulation/demodulation mode. The invention is applicable and directed to other modulation and demodulation modes, such as but not limited to those described herein, as well as frequency hopping according to IEEE 802.11, OFDM (orthogonal frequency division multiplexing), as well as others. These modulation/demodulation modes will be appreciated by persons skilled in the relevant art(s) based on the teachings contained herein.

The operation of the WLAN interface/modem 3902 when receiving shall now be described.

Signals 3922 received by the antenna 3904 are amplified by the LNA/PA 3904. The amplified signals 3924 are down-converted and demodulated by the receiver 3906. The receiver 3906 outputs I signal 3926 and Q signal 3928.

FIG. 40 illustrates an example receiver 3906 according to an embodiment of the invention. It is noted that the receiver 3906 shown in FIG. 40 represents a vector modulator. In an embodiment,

the "receiving" function performed by the WLAN interface/modem 3902 can be considered to be all processing performed by the WLAN interface/modem 3902 from the LNA/PA 3904 to generation of baseband information.

Signal 3924 is split by a 90 degree splitter 4001 to produce an I signal 4006A and Q signal 4006B that are preferably 90 degrees apart in phase. I and Q signals 4006A, 4006B are down-converted by UFD (universal frequency down-conversion) modules 4002A, 4002B. The UDF modules 4002A, 4002B output down-converted I and Q signals 3926, 3928. The UFD modules 4002A, 4002B each includes at least one UFT (universal frequency translation) module 4004A. UFD and UFT modules are described above.

The demodulator/modulator facilitation module 3912 receives the I and Q signals 3926, 3928. The demodulator/modulator facilitation module 3912 optionally amplifies and filters the I and Q signals 3926, 3928. The demodulator/modulator facilitation module 3912 also optionally performs automatic gain control (AGC) functions. The AGC function is coupled with the universal frequency translation technology described herein. The demodulator/modulator facilitation module 3912 outputs processed I and Q signals 3930, 3932.

The MAC interface 3914 receives the processed I and Q signals 3930, 3932. The MAC interface 3914 preferably includes a baseband processor. The MAC interface 3914 preferably performs functions such as combining the I and Q signals 3930, 3932, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface 3914 and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The MAC interface 3914 outputs the baseband information signal, which is received and processed by the computer 3916 in an implementation and application specific manner.

In the example embodiment of FIG. 39, the demodulation function is distributed among the receiver 3906, the demodulator/modulator facilitation module 3912, and a baseband processor contained in the MAC interface 3914. The functions collectively performed by these components include, but are not limited to, de-spreading the information, differentially decoding the information,

tracking the carrier phase, de-scrambling, recreating the data clock, and combining the I and Q signals. The invention is not limited to this arrangement. These demodulation-type functions can be centralized in a single component, or distributed in other ways.

The operation of the WLAN interface/modem 3902 when transmitting shall now be described.

A baseband information signal 3936 is received by the MAC interface 3914 from the computer 3916. The MAC interface 3914 preferably performs functions such as splitting the baseband information signal to form I and Q signals 3930, 3932, and arranging the data according to the protocol/file formal being used. Other functions performed by the MAC interface 3914 and the baseband processor contained therein will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

The demodulator/modulator facilitation module 3912 filters and amplifies the I and Q signals 3930, 3932. The demodulator/modulator facilitation module 3912 outputs processed I and Q signals 3942, 3944. Preferably, at least some filtering and/or amplifying components in the demodulator/modulator facilitation module 3912 are used for both the transmit and receive paths.

The transmitter 3910 up-converts the processed I and Q signals 3942, 3944, and combines the up-converted I and Q signals. This up-converted/combined signal is amplified by the LNA/PA 3904, and then transmitted via the antenna 3904.

FIG. 41 illustrates an example transmitter 3910 according to an embodiment of the invention. The device in FIG. 41 can also be called a vector modulator. The "transmit" function performed by the WLAN interface/modem 3902 can be considered to be all processing performed by the WLAN interface/modem 3902 from receipt of baseband information through the LNA/PA 3904.

I and Q signals 3942, 3944 are received by UFU (universal frequency up-conversion) modules 4102A, 4102B. The UFU modules 4102A, 4102B each includes at least one UFT module 4104A, 4104B. The UFU modules 4102A, 4102B up-convert I and Q signals 3942, 3944. The UFU modules 4102A, 4102B output up-converted I and Q signals 4106, 4108. The 90 degree combiner 4110 effectively phase shifts either the I signal 4106 or the Q signal 4108 by 90 degrees, and then

combines the phase shifted signal with the unshifted signal to generate a combined, up-converted I/Q signal 3946.

In the example embodiment of FIG. 39, the modulation function is distributed among the transmitter 3910, the demodulator/modulator facilitation module 3912, and a baseband processor contained in the MAC interface 3914. The functions collectively performed by these components include, but are not limited to, differentially encoding data, splitting the baseband information signal into I and Q signals, scrambling data, and data spreading. The invention is not limited to this arrangement. These modulation-type functions can be centralized in a single component, or distributed in other ways.

The components in the WLAN interface/modem 3902 are preferably controlled by the MAC interface 3914 in operation with the MAC 3918 in the computer 3916. This is represented by the distributed control arrow 3940 in FIG. 39. Such control includes setting the frequency, data rate, whether receiving or transmitting, and other communication characteristics/modes that will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

FIG. 42 illustrates an example implementation of the WLAN interface/modem 3902. It is noted that in this implementation example, the MAC interface 3914 is located on a different board. FIG. 62 is an example motherboard corresponding to FIG. 42. FIG. 63 is an example bill-of-materials (BOM) list for the motherboard of FIG. 62. This and other implementations are provided herein for example purposes only. Other implementations will be apparent to persons skilled in the relevant art(s), and the invention is directed to such other implementations.

FIG. 102 illustrates an alternate example PCMCIA test bed assembly for a WLAN interface/modem 3902 according to an embodiment of the invention. In this embodiment, the baseband processor 10202 is separate from the MAC interface 3914.

In some applications, it is desired to separate the receive path and the transmit path. FIG. 43 illustrates an example receive implementation, and FIG. 44 illustrates an example transmit implementation.

6.3.2. Receiver

An example implementation of the receiver 3906 (vector demodulator) is shown in FIG. 53. An example BOM list for the receiver 3906 of FIG. 53 is shown in FIG. 54. It is noted that the invention is not limited to this example.

6.3.3. Transmitter

An example implementation of the transmitter 3910 (vector modulator) is shown in FIGS. 57-60. The data conditioning interfaces 5802 in FIG. 58 effectively pre-process the I and Q signals 3942, 3944 before being received by the UFU modules 4102. An example BOM list for the transmitter 3910 of FIGS. 57-60 is shown in FIGS. 61A and 61B. It is noted that the invention is not limited to this example.

6.3.4. Demodulator/Modulator Facilitation Module

An example demodulator/modulator facilitation module 3912 is shown in FIGS. 47 and 48. A corresponding BOM list is shown in FIGS. 49A and 49B.

An alternate example demodulator/modulator facilitation module 3912 is shown in FIGS. 50 and 51. A corresponding BOM list is shown in FIGS. 52A and 52B. It is noted that the invention is not limited to this example.

6.3.5. MAC Interface

An example MAC interface 3914 is shown in FIG. 45. A corresponding BOM list is shown in FIGS. 46A and 46B. It is noted that the invention is not limited to this example.

6.3.6. Control Signal Generator - Synthesizer

In an embodiment, the control signal generator 3908 is preferably implemented using a synthesizer. An example synthesizer is shown in FIG. 55. A corresponding BOM list is shown in FIGS. 56A and 56B. It is noted that the invention is not limited to this example.

6.3.7. LNA/PA

An example LNA/PA 3904 is shown in FIGS. 64 and 65. A corresponding BOM list is shown in FIG. 66. It is noted that the invention is not limited to this example.

6.3.8. Test Results

Test results relating to the operation of the WLAN interface/modem 3902 are shown in FIGS. 67-70, 90-94, and 151-169. FIGS. 95-100 relate to IIP2 and IIP3, and FIG. 101 relates to power consumption. It is noted that the invention is not limited to this example.

6.4 IEEE Standard 802.11 Background

Embodiments of the present invention shall now be described in greater detail. It is noted that these embodiments are described herein for illustrative purposes only. The invention is not limited to these embodiments. Other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

IEEE Std 802.11-1997 defines a medium access control (MAC) sublayer, MAC management protocols and services, and three physical (PHY) layers. The three PHY layers are an infrared (IR) baseband PHY, a frequency hopping spread spectrum (FHSS) radio in the 2.4 GHz band, and a direct sequence spread spectrum (DSSS) radio in the 2.4 GHz band. All three physical layers describe both

1 and 2 Mbps operation. The universal frequency translation techniques of the present invention are applicable to these physical layers.

Two further PHY layers are IEEE Std 802.11a and IEEE Std 802.11b. IEEE Std 802.11a is an orthogonal frequency domain multiplexing (OFDM) radio in the UNII bands, delivering up to 54 Mbps data rates. The second, IEEE Std 802.11b, is an extension to the DSSS PHY in the 2.4 GHz band, delivering up to 11 Mbps data rates. The present invention is also applicable to these physical layers.

The IEEE 802.11 standard describes a WLAN that delivers services similar to those found in wired networks, including high throughput, highly reliable data delivery, and continuous network connections. In addition, IEEE 802.11 describes a WLAN that allows transparent mobility and built-in power saving operations to the network user. The subsections that follow describe the architecture of the IEEE 802.11 network, concepts related to supporting the architecture, and applications of universal frequency translation in the IEEE 802.11 network architecture.

Further details on designing, configuring, and operating WLANs and WLAN stations according to IEEE Standard 802.11 are provided in a number of publicly available documents, such as Bob O'Hara & Al Petrick, "IEEE 802.11 Handbook: A Designer's Companion" (1999) (hereinafter IEEE 802.11 Handbook), which is incorporated herein by reference in its entirety.

6.4.1 IEEE 802.11 Architecture

An IEEE 802.11 WLAN provides a network where most decision making is distributed to mobile stations. This provides several advantages, including being tolerant of faults in WLAN equipment and eliminating bottlenecks that may be present in a centralized architecture. The IEEE 802.11 WLAN architecture is very flexible, supporting small, transient networks and large semipermanent or permanent networks. Deep power-saving modes of operation are built into the architecture, along with protocols to prolong the battery life of mobile equipment without losing network connectivity. These advantages of the IEEE 802.11 WLAN architecture may be enhanced

by the incorporation of universal frequency translation technology of the present invention. An IEEE 802.11 architecture environment may comprise several components. These may include: the station, the access point (AP), the wireless medium, the basic service set, the distribution system (DS), and the Extended Service Set. The architecture may also include station services and distribution services.

The IEEE 802.11 WLAN architecture also embeds a level of indirection that has not been present in previous LANs. This level of indirection, transparent to protocol users of the IEEE 802.11 WLAN, allows a mobile station to roam throughout a WLAN while appearing to be stationary to protocols above the MAC that have no concept of mobility. This ability allows all of the existing network protocols to run over a WLAN without any special considerations.

6.4.1.1 The Station

The station connects to the wireless medium. The station includes a MAC and a PHY. In embodiments, the station may be referred to as the network adapter or network interface card (NIC), as known to persons skilled in the relevant art(s) from the teachings herein.

The station may be mobile, portable, or stationary. Every station supports station services. These services include authentication, de-authentication, privacy, and delivery of the data (MAC service data unit or MSDU in the standard). Station services are further described elsewhere herein. Embodiments of WLAN stations incorporating universal frequency translation technology of the present invention are presented further below.

6.4.1.2 The Basic Service Set

A basic service set (BSS) is a set of stations that communicate with one another. When all stations in a BSS are mobile stations, and there is no connection to a wired network, the BSS may be referred to as an independent BSS (IBSS). An IBSS is an entire network. Only those stations

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communicating with each other in the IBSS are part of the LAN. An IBSS may be a short-lived network, with a small number of stations, that is created for a particular purpose.

Mobile stations within an IBSS communicate directly with one another. Not every mobile station within an IBSS may be able to communicate with every other mobile station, but they are all part of the same IBSS. There is no relay function in an IBSS. Thus, if one mobile station must communicate with another, they must be in direct communication range. FIG. 124 illustrates an IBSS 12400 with mobile stations that must be in direct communication range to communicate with each other.

When a BSS includes an access point (AP), the BSS is no longer independent. It may then be referred to as an infrastructure BSS, or simply a BSS. An AP is a station that also provides distribution services. Distribution services are further described elsewhere herein.

In an infrastructure BSS, all mobile stations communicate with the AP. The AP provides both a connection to a wired LAN, if one exists, and a local relay function for the BSS. For example, if one mobile station in a BSS must communicate with another mobile station within the BSS, the communication is sent first to the AP, and then from the AP to the other mobile station. Hence, communications that both originate and end in the same BSS may consume twice the bandwidth as direct communications from one mobile station to another. FIG. 101A illustrates an IBSS 10100 with mobile stations that communicate through an AP 10102. A benefit provided by an AP is the buffering of traffic for a mobile station while that station is operating in a very low power state. Protocols and mechanisms supporting power saving by mobile stations are further described elsewhere herein. An AP may incorporate universal frequency translation technology to provide for the AP's relay communication function. FIG. 101B illustrates an AP 10102 that includes a universal frequency translation module 10204, according to an embodiment of the present invention. The embodiments presented herein for receiving and transmitting WLAN signals by WLAN stations are applicable to APs.

6.4.1.3 Extended Service Set (ESS)

A benefit provided by a WLAN is the mobility it provides to its users. This mobility is not confined to a single BSS. IEEE 802.11 extends the range of mobility to any arbitrary range through an extended service set (ESS). An ESS is a set of two or more infrastructure BSSs. In an ESS, APs communicate among themselves to forward traffic from one BSS to another, and to facilitate the movement of mobile stations from one BSS to another. The APs perform this communication via an abstract medium called the distribution system (DS). The DS is a backbone of the WLAN and may be constructed of either wired or wireless networks. The DS is a thin layer in each AP that determines whether communications received from the BSS are to be relayed back to a destination in the BSS, forwarded on the DS to another AP, or sent into the wired network infrastructure to a destination not in the ESS. Communications received by an AP from the DS are transmitted to the BSS to be received by the particular destination mobile station. To network equipment outside of the ESS, the ESS and all of its mobile stations appears to be a single MAC-layer network where all stations are physically stationary. Thus, the ESS hides the mobility of the mobile stations from everything outside the ESS. The IEEE 802.11 architecture provides this level of indirection, allowing existing network protocols that have no concept of mobility to operate correctly with a WLAN where mobility exists. FIG. 125 illustrates an exemplary ESS 12500.

6.4.1.4 Distribution System

The distribution system (DS) allows an AP to communicate with another AP. The APs may exchange frames for stations in their BSSs, forward frames to follow mobile stations from one BSS to another, and exchange frames with wired networks, if any. As set forth by IEEE 802.11, the DS is not necessarily a network. The standard does not place any restrictions on how the DS is implemented, only on the services it must provide. Thus, the DS may be a wired network, for

example, such as IEEE 802.3, or it may be an application specific box that interconnects the AP, and provides the required distribution services.

6.4.1.5 IEEE 802.11 Services

There are nine services defined by the IEEE 802.11 architecture. These services may be divided into two groups: station services and distribution services. Station services comprise authentication, de-authentication, privacy, and delivery of the data. Distribution services comprise association, disassociation, re-association, distribution, and integration.

6.4.1.5.1 Station Services

Four station services - authentication, de-authentication, privacy, and data delivery -provide a IEEE 802.11 WLAN with functions similar to those expected of a wired network. The physical network cable connection of a wired network is similar to the authentication and de-authentication services, where use of the network is limited to authorized users. The authentication service is used to prove the identity of one station to another. Without this proof of identity, the station is not allowed to use the WLAN for data delivery. The de-authentication service is used to eliminate a previously authorized user from any further use of the network. Thus, once a station is de-authenticated (for example, when an employee resigns) that station can no longer access the services of the IEEE 802.11 WLAN.

The privacy service of IEEE 802.11 is designed to provide an equivalent level of protection for data traversing the WLAN as is provided by a wired network that exists in an office building with restricted physical access to the network plant. This service protects the data only as it traverses the wireless medium. It is not designed to provide complete protection of data between applications running over a mixed network environment that happens to include an IEEE 802.11 WLAN.

Finally, the data delivery service of an IEEE 802.11 WLAN is similar to that provided by all other IEEE 802.11 LANs. The data delivery service provides reliable delivery of data frames from a MAC in a first station to a MAC in one or more further stations, with minimal duplication and minimal reordering.

6.4.1.5.2 Distribution Services

Five distribution services - association, re-association, disassociation, distribution, and integration - provide services necessary to allow mobile stations to roam freely within an ESS, and to allow an IEEE 802.11 WLAN to connect with a wired LAN infrastructure. The distribution services comprise a thin layer above the MAC and below the logical link control (LLC) sublayer. The distribution services may be invoked to determine how to forward frames within an IEEE 802.11 WLAN, and to determine how to deliver frames from a IEEE 802.11 WLAN to network destinations outside of the WLAN.

The association service is used to make a logical connection between a mobile station and an AP. This logical connection allows for the DS to know where and how to deliver data to the mobile station. The logical connection allows the AP to accept data frames from the mobile station and to allocate resources to support the mobile station. Typically, the association service is invoked once, when the mobile station enters the WLAN for the first time, such as after the application of power, or when rediscovering the WLAN after being out of touch for a time.

The re-association service is similar to the association service, with a difference that it includes information about the AP with which a mobile station has been previously associated. A mobile station may use the re-association service repeatedly as it moves throughout an ESS. For instance, the mobile station may lose contact with an AP with which it is associated, and may need to become associated with a new AP. Through the re-association service, a mobile station provides information to an AP to which it will become associated. This information allows the AP to contact the AP previously associated with the mobile station. The previously associated AP may be

contacted to obtain frames that may be waiting there for delivery to the mobile station, as well as other information that may be relevant.

The disassociation service may be used to force a mobile station to disassociate. An AP may inform one or more mobile stations that the AP can no longer provide the logical connection to the WLAN. This may be due to the available resources in the AP being exceeded, the AP shutting down, or other reasons. When the mobile station becomes disassociated, it may begin a new association by invoking the association service.

A mobile station may also use the disassociation service. When a mobile station is aware that it will no longer require the services of an AP, it may invoke the disassociation service to notify the AP that the logical connection to the WLAN is not required. For example, this may occur when the mobile station is being shut down, or when the IEEE 802.11 adapter card is being ejected. Once the mobile station is disassociated, an AP may recover any resources dedicated to the mobile station for other uses.

When determining how to deliver the frames it receives, an AP uses the distribution service. When a mobile station sends a frame to an AP for delivery to another station, the AP invokes the distribution service to determine where to send the frame. It must be determined if the frame should be sent back into its own BSS for delivery to a mobile station associated with the AP, if the frame should be sent into the DS for delivery to another mobile station associated with a different AP, or if the frame should be sent to a network destination outside the IEEE 802.11 WLAN. The distribution service determines whether the frame is sent to another AP or to a portal.

The integration service couples the IEEE 802.11 WLAN to other LANs, including possibly one or more wired LANs, or other IEEE 802.11 WLANs. A portal performs the integration service. The portal is an abstract architectural concept and may physically reside as a thin layer in some or all APs, or may be a separate network component entirely. The integration service translates IEEE 802.11 frames into frames that may traverse another network. The integration service also translates frames from other network types to frames that may be delivered by an IEEE 802.11 WLAN.

6.4.1.5.3 Service Interaction

The IEEE 802.11 standard states that each station must maintain two variables that are dependent on the authentication/de-authentication services and the association/re-association/ disassociation services. The two variables are authentication state and association state. While the standard describes these variables as being enumerated types, they are typically available internal to an implementation, and may be implemented as Boolean truth-values. The variables may be used in a simple state machine that determines the order in which certain services may be invoked and when a station may begin using the data delivery service. The variables must exist in enough instances to allow the station to maintain a unique copy for each station with which it communicates. A station may be authenticated with many different stations simultaneously. However, a station may be associated with only one other station at a time.

FIG. 126 illustrates a state diagram 12600 showing the relationship between state variables and services. A station begins operation in a first state, state 12602, where both authentication state and association state are false, indicating that the station is neither authenticated nor associated. In state 12602, a station may use a very limited number of frame types, which are more fully described below. The allowable frame types provide the capability for a station in state 12602 to find an IEEE 802.11 WLAN, an ESS, and its APs, to complete the required frame handshake protocols, and to implement the authentication service. If a station is not successful in becoming authenticated, it will remain in state 12602. If a station becomes authenticated, authentication state is set to true, and the station will make a transition to a state 12604. This transition is shown in FIG. 126 as transition 12608.

If a station is part of an IBSS, it may implement the data service in state 12602. This is because neither authentication nor association are used in an IBSS, leaving no mechanism for a station in an IBSS to leave state 12602.

In the second state, state 12604, the station has been authenticated. This is indicated by the authentication state being true. In state 12604, however, the station has not yet associated. In state

12604, additional frame types are allowed, beyond those allowed in state 12602. The additional frame types provide the capability for a station in state 12604 to implement the association, re-association, and disassociation services. If a station is not successful in becoming associated, it will remain in state 12604, unless it receives a de-authentication notification. If it receives a de-authentication notification, it will return to state 12602 via a transition 12610, and authentication state will be made false. If a station becomes associated, setting association state to true, it will travel along a transition 12612 to a state 12606.

In the third state, state 12606, the station has been both authenticated and associated, indicated by both authentication state and association state being true. In this state, all frame types are allowed and the station may use the data delivery service. A station will remain in state 12606 until receiving either a disassociation notification or a de-authentication notification, or until it re-associates with another station. If a station receives a disassociation notification, it will travel along a transition 12614 to state 12604 and set association state to false. If a station receives a de-authentication notification, it will travel along a transition 12616 to state 12602 and set both authentication state and association states to false.

A station must react to frames it receives in each of the states, even those frames that are disallowed for a particular state. A station will send a de-authentication notification to any station with which it is not authenticated if it receives frames that are not allowed in state 12602. A station will send a disassociation notification to any station with which it is authenticated, but not associated, if it receives frames not allowed in state 12604. These notifications will force the station that sent the disallowed frames to make a transition to the proper state, allowing it to proceed properly toward state 12606.

A station may make many transitions between states of state diagram 12600 shown in FIG. 126 as it roams through an ESS. Because a station may be authenticated with many stations at once, it may be in state 12604 with relation to those stations. However, a station may be in state 12606 with relation to a different station. When a station re-associates with another station, the station with

which it was previously associated must be moved back to state 12604, setting the value of associated state for that station to false.

FIG. 127 illustrates a station 12702 moving between APs. As the station 12702 finds a first AP, AP 12704, it will authenticate and associate (a). As station 12702 moves, it may pre-authenticate with a second AP, AP 12706 (b). When the station 12702 determines that its association with AP 12704 is no longer desirable, it may re-associate with AP 12706 (c). The re-association with AP 12706 causes AP 12706 to notify AP 12704 of the new location of station 12702, terminating the previous association of station 12702 with AP 12704 (d). At some point, AP 12706 may be taken out of service. If this occurs, AP 12706 disassociates the stations that were associated with it (e). This would require station 12702 to find another access point, AP 12708, and to authenticate and associate, in order to continue using the wireless LAN (f).

The architecture and services of IEEE 802.11 allow a WLAN to appear similar to wired LANs. The architecture divides the functionality of the WLAN into non-overlapping functional blocks. The services described by IEEE 802.11 provide the user of IEEE 802.11 with the functionality of a wired LAN and the additional benefits of mobility.

6.5 Medium Access Control Overview

The IEEE 802.11 medium access control (MAC) supplies the functionality required to provide a reliable delivery mechanism for user data over potentially noisy, unreliable wireless media. The MAC does this while also providing advanced LAN services, equal to or beyond those of wired LANs.

6.5.1 MAC Functionality

A first function of the MAC is to provide a reliable data delivery service to users of the MAC. Through a frame exchange protocol at the MAC level, the IEEE 802.11 MAC improves on the reliability of data delivery over wireless media, as compared to earlier WLANs.

A second function of the IEEE 802.11 MAC is to control access to the shared wireless medium. It performs this function through two different access mechanisms: the basic access mechanism, known as the distributed coordination function, and a centrally controlled access mechanism, known as the point coordination function.

A third function of the IEEE 802.11 MAC is to protect the data that it delivers. Because a WLAN generally is not limited to a particular physical area, the IEEE 802.11 MAC provides a privacy service, called Wired Equivalent Privacy (WEP), which encrypts the data sent over the wireless medium. The level of encryption chosen may approximate the level of protection that data may have on a wired LAN that does not allow a physical connection to LAN wiring without authorization.

6.5.2 MAC Frame Exchange Protocol

Because the media used by the IEEE 802.11 WLAN are often very noisy and unreliable, the IEEE 802.11 MAC implements a frame exchange protocol to allow the source of a frame to determine when the frame has been successfully received at the destination. This frame exchange protocol adds some overhead beyond that of other MAC protocols, like IEEE 802.3, because it is not sufficient to simply transmit a frame and expect that the destination has received it correctly on wireless media. In addition, every station in a WLAN cannot necessarily communicate directly with every other station in the WLAN. This leads to a situation known as the hidden node problem. The MAC frame exchange protocol is also designed to address this problem of WLANs. The frame

exchange protocol requires the participation of all stations in the WLAN. For this reason, every station decodes and reacts to information in the MAC header of every frame it receives.

6.5.2.1 Handling the Media

The minimal MAC frame exchange protocol consists of two frames: a frame sent from the source to the destination, and an acknowledgment from the destination that the frame was received correctly. The frame and its acknowledgment are an atomic unit of the MAC protocol. As such, they cannot be interrupted by the transmission from any other station.

The destination may not send an acknowledgment because of errors in the original frame, or because the acknowledgment itself was corrupted. If the source does not receive the acknowledgment, the source will attempt to transmit the frame again, according to the rules of the basic access mechanism described below. This retransmission of frames by the source effectively reduces the inherent error rate of the medium, with the cost of additional bandwidth consumption. Without this mechanism for retransmission, the users of the MAC, i.e., higher layer protocols, would be left to determine that their packets had been lost through higher layer timeouts or other means. Since higher layer timeouts are often measured in seconds, it is much more efficient to deal with this issue at the MAC layer.

6.5.2.2 The Hidden Node Problem

A WLAN may suffer from a problem that does not occur on a wired LAN. The problem is one of "hidden nodes." This is a result of the fact that every WLAN station cannot be expected to communicate directly with every other WLAN station. The following example illustrates this problem.

In this example, there are three stations, A, B, and C, arranged as shown in FIG. 67. Station A can communicate only with station B. Station B can communicate with stations A and C. Station

C can communicate only with station B. If a simple "transmit and hope" protocol were to be used when station A was sending a frame to station B, the frame could be corrupted by a transmission begun by station C. Station C would be completely unaware of the ongoing transmission from station A to station B.

The IEEE 802.11 MAC frame exchange protocol addresses this problem by adding two additional frames to the minimal frame exchange protocol described so far. The two frames are a request to send frame and a clear to send frame. The source sends a request to send to the destination. The destination returns a clear to send to the source. Each of these frames contain information that allows other stations receiving them to be notified of the upcoming frame transmission and to delay any transmissions of their own. The request to send and clear to send frames serve to announce to all stations in the neighborhood of both the source and destination the impending transmission from the source to the destination. When the source receives the clear to send from the destination, the real frame that the source wants delivered to the destination is sent. If that frame is correctly received at the destination, the destination will return an acknowledgment, completing the frame exchange protocol. Depending on the configuration of a station and its determination of local conditions, a station may choose when to use the request to send and clear to send frames. See FIG. 68.

The four frames in this exchange are also an atomic unit of the MAC protocol. They cannot be interrupted by the transmissions of other stations. If this frame exchange fails at any point, the state of the exchange and the information carried in each of the frames allows the stations that have received these frames to recover and regain control of the medium in a minimal amount of time. A station in the neighborhood of the source station receiving the request to send frame will delay any transmissions of its own until it receives the frame announced by the request to send. If the announced frame is not detected, the station may use the medium. Similarly, a station in the neighborhood of the destination station receiving the clear to send frame will delay any transmissions of its own until it receives the acknowledgment frame. If the acknowledgment frame is not detected, the station may use the medium.

In the source station, a failure of the frame exchange protocol causes the frame to be retransmitted. This is treated as a collision, and the rules for scheduling the retransmission are described in the section on the basic access mechanism, below. To prevent the MAC from being monopolized attempting to deliver a single frame, there are retry counters and timers to limit the lifetime of a frame.

While this four-way frame exchange protocol is a required function of the MAC, it may be disabled by an attribute in the management information base (MIB). The value of the dot11RTSThreshold attribute defines the length of a frame that is required to be preceded by the request to send and clear to send frames. All frames of a length greater than the threshold will be sent with the four-way frame exchange. Frames of a length less than or equal to the threshold will not be preceded by the request to send and clear to send. This allows a network designer to tune the operation of the IEEE 802.11 WLAN for the particular environment in which it is deployed. In an environment with low demand for bandwidth or where the stations are concentrated in an area where all are able to receive the transmissions of every station, the threshold may be set so that the request to send and clear to send are never used. As long as stations are not contending with each other, the request to send and clear to send frames will most often be consuming bandwidth for no measurable gain. This is the default setting for the threshold. In an environment where there is a significant demand for the bandwidth available in the WLAN or where the stations are distributed such that some may not hear the transmission of others, the threshold may be set lower, causing long frames to use the request to send and clear to send frame exchange. The value to which the threshold should be set is arrived at by comparing the bandwidth lost to the additional overhead of the protocol to the bandwidth lost from transmissions being corrupted by hidden nodes. A typical value for the threshold is 128. However, the value chosen is dependent on the data rate and should be calculated for the particular data rate in use. It is rarely necessary to change the value of dot11RTSThreshold from the default value in an AP. By definition, an AP is heard by all stations in its BSS and will never be a hidden node. The only situation that may warrant changing the value for the RTS threshold in an AP is when APs are co-located and sharing a channel.

Timing intervals are described in the following subsection. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on MAC frame exchange protocol.

6.5.2.3 Timing Intervals

The decision by a station that the medium in not carrying a transmission when the station is listening before beginning its own transmission is based on timing intervals. The IEEE 802.11 MAC recognizes five timing intervals. There are two basic intervals determined by the PHY: the short interframe space (SIFS) and the slot time. Three additional intervals are built from the two basic intervals: the priority interframe space (PIFS), the distributed interframe space (DIFS), and the extended interframe space (EIFS). The SIFS is the shortest interval, followed by the slot time, which is slightly longer. The PIFS is equal to SIFS plus one slot time. The DIFS is equal to the SIFS plus two slot times. The EIFS is much larger than any of the other intervals. It is used when a frame that contains errors is received by the MAC, allowing the possibility from the MAC frame exchanges to complete correctly before another transmission is allowed. Through these five timing intervals, both the distributed coordination function (DCF) and point coordination function (PCF) are implemented.

6.5.3 Frame Formats

The IEEE 802.11 MAC accepts MSDUs from higher layers in the protocol stack for the purpose of reliably sending those MSDUs to the equivalent layer of the protocol stack in another station. To accomplish this task, the MAC adds information to the MSDU in the form of headers and trailers to create a MAC protocol data unit (MPDU). The MPDU is then passed to the physical layer to be sent over the wireless medium to the other stations. In addition, the MAC may fragment MSDUs into several frames, increasing the probability of each individual frame being delivered successfully. A discussion of fragmentation follows the description of frame formats in this chapter.

The header and trailer information, combined with the information received as the MSDU, is referred to as the MAC frame. This frame contains, among other things, addressing information, IEEE 802.11-specific protocol information, information for setting the NAV, and a frame check sequence for verifying the integrity of the frame. Further details of the frame format are presented in the following sections.

6.5.3.1 General Frame Format

The general IEEE 802.11 frame format is shown in FIG. 69. This frame format is quite a bit more complex than that for most other LAN protocols. The frame begins with a MAC header. The start of the header is the frame control field. A field that contains the duration information for the NAV or a short identifier follows it. Three addressing fields follow that field. The next field contains frame sequence information. The final field of the MAC header is the fourth address field. It may appear that the MAC header is very long. However, not all of these fields are used in all frames.

Following the MAC header is the frame body. The frame body contains the MSDU from the higher layer protocols. The final field in the MAC frame is the frame check sequence.

Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on each of the general frame format fields, and their use in particular frame types.

6.5.4 Control Frame Subtypes

There are six control frame subtypes: request to send (RTS), clear to send (CTS), acknowledge (ACK), power save poll (PS-Poll), contention-free end (CF-End), and contention-free end plus ACK (CF-End+ACK). A description of these frames follows.

6.5.4.1 Request to Send

The request to send (RTS) frame is 20 bytes in length. It comprises the frame control field, the duration/ID field, two address fields and the frame check sequence field. The purpose of this frame is to transmit the duration information to those stations in the neighborhood of the transmitter, in order that the stations receiving the RTS frame will update their NAV to prevent transmissions from colliding with the data or management frame that is expected to follow. The RTS is also the first frame in a four-way frame exchange handshake between the transmitter and the receiver. See FIG. 70.

The RA identifies the individual MAC that is the immediate intended recipient of the frame. In an RTS frame, the RA is always an individual address. The TA identifies the source of the transmission. It is used by the station addressed by the RA to form the clear to send (CTS) frame that is the response to the RTS. The duration information conveyed by this frame is a measure of the amount of time required to complete the four-way frame exchange. The value of the duration is the length of time to transmit a CTS, the data or management frame, the acknowledge (ACK) frame, and the two SIFS intervals between the CTS and the data or management frame and between the data or management frame and the ACK. The duration is measured in microseconds. Fractional microseconds are always rounded up to the next larger integer value.

6.5.4.2 Clear to Send

The clear to send (CTS) frame is 14 bytes in length. It comprises the frame control field, the duration/ID field, one address field, and the frame check sequence field. The purpose of this frame is to transmit the duration information to those stations in the neighborhood of the station intended to receive the expected data or management frame, in order that the stations receiving the CTS frame will update their NAV to prevent transmissions from colliding with the data or management frame

that is expected to follow. The CTS is the second frame in a four-way frame exchange handshake between the transmitter and the receiver. See FIG. 90.

The RA identifies the individual MAC address of the station to which the CTS is sent. In the CTS frame, the RA is always an individual address.

The RA value is taken directly from the TA of the preceding RTS frame. The duration information conveyed by this frame is a measure of the time required to complete the four-way frame exchange handshake. The value of the duration is the length of time to send the subsequent data or management frame, the acknowledge frame, and one SIFS interval. The duration value is calculated by subtracting the length of time to transmit a CTS and one SIFS interval from the duration that was received in the WFS frame. The duration is measured in microseconds. Fractional microseconds are always rounded up to the next larger integer value.

6.5.4.3 Acknowledge

The acknowledge (ACK) frame is 14 bytes in length. It comprises the frame control field, the duration/ID field, one address field and the frame check sequence field. The purpose of this frame is two-fold. First, the ACK frame transmits an acknowledgment to the sender of the immediately previous data, management, or PS-Poll frame that the frame was received correctly. This informs the sender of the frame of the frame's receipt and eliminates the requirement for retransmission by the sender. Second, the ACK frame is used to transmit the duration information for a fragment burst to those stations in the neighborhood of the station intended to receive the fragments. In this case, it performs exactly as the CTS frame. The ACK frame is the fourth frame in the four-way frame exchange handshake between transmitter and receiver. See FIG. 91.

The RA identifies the individual MAC address of the station to which the ACK is sent. In the ACK frame, the RA is always an individual address. The RA value is taken directly from the address 2 field of the immediately preceding data, management, or PS-Poll frame.

The value of the duration information is zero, if the ACK is an acknowledgment of a PS-Poll frame or is an acknowledgment of a management or data frame where the more fragments subfield of the frame control field is zero. The value of the duration information is the time to transmit the subsequent data or management frame, an ACK frame, and two SIFS intervals, if the acknowledgment is of a data or management frame where the more fragments subfield of the frame control field is one. In the latter case, the duration may be calculated by subtracting the length of time to transmit the ACK frame and one SIFS interval from the duration value received in the immediately preceding data or management frame. The duration value is measured in microseconds. Fractional microseconds are always rounded up to the next integer value.

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6.5.4.4 Power Save Poll

The power save poll (PS-Poll) frame is 20 bytes in length. It comprises the frame control field, the duration/ID field, two address fields, and the frame check sequence field. The purpose of this frame is to request that an AP deliver a frame that has been buffered for a mobile station while it was in a power saving mode.

The BSSID identifies the AP to which this frame is directed. This BSSID should be the same BSSID as that to which the sending station has previously associated. The BSSID in the PS-Poll frame is always an individual address. The TA is the MAC address of the mobile station that is sending the PS-Poll frame. The duration/ID value is the AID value that was given to the mobile station upon association with the BSS. Even though this frame does not include any explicit duration information, every mobile station receiving a PS-Poll frame will update its NAV with a value which is the length of time to transmit an ACK frame and a single SIFS interval. This action allows the ACK frame that follows the PS-Poll to be sent by the AP with a very small probability. that it will collide with frames from mobile stations.

For the AP response to this frame, refer to Chapter 4 of the IEEE 802.11 Handbook.

6.5.4.5 CF-End and CF-End+ACK

The CF-End and CF-End+ACK frames are 20 bytes in length. Each frame comprises the frame control field, the duration/ID field, two address fields, and the frame check sequence field. The purpose of these frames is to conclude a CFP and to release stations from the restriction imposed during a CFP, preventing competition for access to the medium. Additionally, the CF-End+ACK frame is used to acknowledge the last transmission received by the PC. This frame is sent by the PC as the last frame in the CFP.

The RA is the broadcast group address, as this frame is intended to be received by every station in the BSS. The BSSID is the MAC address of the AP, where the PC resides. The duration value is zero, ensuring that the NAVs of all stations receiving this frame will be reset to zero.

6.5.5 Data Frame Subtypes

There are eight data frame subtypes in two groups. The first group is simple data, data with contention-free acknowledgment (CF-ACK), data with CF-Poll, and data with CF-ACK and CF-Poll. The second group is null function, CF-ACK, CF-Poll, and CF-ACK+CF-Poll. The first group of data frames carry a nonzero number of data bytes. The second group of data frames carry no data bytes at all.

The data frame is variable in length. The minimum length of the data frame is 29 bytes. The maximum length of the frame is 2346 bytes. The data frame carries the MSDU requested to be delivered by the upper layer protocols. It comprises the frame control field, the duration/ID field, up to four address fields, the sequence control field, the frame body field and the frame check sequence field. See FIG. 92 for a data frame. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on the data frame.

6.5.6 Management Frame Subtypes

IEEE 802.11 is different from many of the other IEEE 802 standards because it includes very extensive management capabilities defined at the MAC level. One of the four MAC frame types is dedicated to management frames. There are 11 distinct management frame types. All management frames include: frame control, duration, address 1, 2, and 3, sequence control, framebody and frame check sequence (FCS) fields.

The frame body of a management frame carries information in both fixed fields and in variable length information elements that are dependent on subtype. The information element is a flexible data structure that contains an information element identifier, a length, and the content of the information element. Information elements occur in the frame body in order of increasing identifiers. This arrangement and the data structure itself allow for the flexible extension of the management frames to include new functionality without affecting older implementations. This can be done because older implementations will be able to understand the older elements and will ignore elements with new identifiers. Because the length of the element is part of the data structure, an older implementation can skip over newer elements without needing to understand the content of the element. See FIG. 93 for an information element. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on the fixed fields and information elements.

6.5.7 Components of the Management Frame Body

The components of the management frame body comprise fixed fields and variable length information elements. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on these fixed fields and information elements.

6.5.8 MAC Management

IEEE 802.11 is the first LAN standard by the IEEE 802 committee that includes significant management capabilities. This is because an IEEE 802.11 WLAN must deal with an environment that is measurably more complex than those of the wired LAN standards of IEEE 802. A major challenge for the IEEE 802.11 WLAN is that the medium is not a wire. This leads to many difficulties that IEEE 802.11 must overcome in order to offer the same reliable service expected of an IEEE 802 LAN.

Because the media over which the IEEE 802.11 WLAN operate are not wires, the media are shared by other users that have no concept of data communication or sharing the media. An example of this type of user is the common microwave oven. The microwave oven operates in the 2.4 GHz ISM band because one excitation frequency of the water molecule lies in this band. Another user in this same band is the radio frequency ID (RFID) tag. RFID tags are usually small, cheap, unpowered devices that receive their power from a microwave beam and then return a unique identifier. RFID tags are used to track retail inventory, identify rail cars, and many other uses. An unfortunate consequence of these devices sharing the band with WLANs is that some of this microwave energy leaks from the oven and is purposely broadcast for RFID tags, thus, interfering with the operation of the WLAN.

There are also other WLANs than IEEE 802.11 that share the media. This would be somewhat equivalent to attempting to run IEEE 802.3, IEEE 802.5, IEEE 802.12, and fiber distributed data interference (FDDI) on the same twisted pair cable, simultaneously. These other WLAN users of the media are often uncoordinated with IEEE 802.11 and, in most cases, do not provide for any mechanism to share the media at all. Finally, there are other IEEE 802.11 WLANs sharing the media.

These other users of the media result in a first challenge for the IEEE 802.11 WLAN, an intermittent connection to the media and other stations of the IEEE 802.11 WLAN. Much of the management specified in IEEE 802.11 is to deal with the intermittent nature of the media.

A second challenge to be dealt with by an IEEE 802.11 WLAN is that anyone can "connect" to the WLAN, simply by erecting the proper antenna. This leads to the need to identify the stations connecting to the WLAN, in order to allow only authorized stations to use the WLAN, and to the need to protect the information sent over the WLAN from improper interception.

A third challenge to be dealt with by an IEEE 802.11 WLAN is mobility. Once the wires are removed from a LAN, the natural thing to do is to pick up the equipment connected to the LAN and move it around, taking it from an office to a conference room or to another building. Thus, IEEE 802.11 equipment is not always in the same place from one moment to the next. Even if the equipment were to remain in a fixed location, the nature of the wireless media may make it appear as if the equipment has moved. Dealing with mobility while making all of the expected LAN services available is a problem to be solved by MAC management.

One final challenge to be dealt with by an IEEE 802.11 WLAN is power management. A consequence of doing away with wired media and enabling the equipment to be mobile is that much of the equipment will be run on batteries. Conserving the energy stored in the batteries to allow the equipment to operate for as long as possible must be built into the WLAN protocol and controlled by MAC management.

6.5.8.1 Tools Available to Meet the Challenges

The IEEE 802.11 standard defines a number of MAC management capabilities that are designed to meet the challenges of operating a reliable WLAN. These tools are: authentication, association, address filtering, privacy, power management, and synchronization. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on each of these tools.

6.5.9 MAC Management Information Base

The IEEE 802.11 management information base (MIB) is an SMNPv2 managed object that contains a number of configuration controls, option selectors, counters, and status indicators that allow an external management agent to determine the status and configuration of an IEEE 802.11 station, as well as to probe its performance and tune its operation. The MIB in a station comprises two major sections, one for the MAC and one for the PHY. The PHY section is subdivided into pieces that are specific to each PHY layer. In the MIB definition, there is also a compliance section that describes the required portions of the MIB and those parts that are optional. All of the attributes are arranged in tables, coordinating the attributes that are related to a single function.

The MAC MIB comprises two sections: the station management attributes and the MAC attributes. The station management attributes are associated with the configuration of options in the MAC and the operation of MAC management. The MAC attributes are associated with the operation of the MAC and its performance.

6.5.9.1 Station Management Attributes

The station management attributes configure and control the operation of the options of the IEEE 802.11 MAC, as well as assist in the management of the station. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on these attributes.

6.5.9.2 MAC Attributes

The MAC attributes tune the performance of the MAC protocol, monitor the performance of the MAC, identify the multicast addresses that the MAC will receive, and provide identification of the MAC implementation. Refer to Chapter 3 of the IEEE 802.11 Handbook for further details on these attributes.

6.6 Physical Layer (PHY)

Embodiments of the PHY are provided in the following sections for receiving, transmitting, modulating, and/or demodulating WLAN signals, according to the present invention. These embodiments are applicable to WLAN stations, APs, and further WLAN related communications components. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.6.1 PHY Functionality

At the bottom of the OSI stack is the PHY. FIG. 128A illustrates an OSI model 12800 including the PHY layer 12802. The PHY 12802 is an interface between the MAC 12804 and wireless media. The PHY 12802 transmits and receives data frames over the shared wireless media. The PHY 12802 provides three levels of functionality. First, the PHY layer 12802 provides a frame exchange between the MAC 12804 and PHY 12802 under the control of a physical layer convergence procedure (PLCP) sublayer 12806. Second, the PHY 12802 uses signal carrier and spread spectrum modulation to transmit data frames over the media under the control of a physical medium dependent (PMD) sublayer 12808. Third, the PHY 12802 provides a carrier sense indication back to the MAC 12804 to verify activity on the media.

The PHY layers are unique in terms of modulation type, coexist with the other PHYs, and operate with the MAC described above. The specifications for IEEE 802.11 were selected to meet the radio frequency (RF) emissions guidelines specified by the Federal Communications Commission (FCC), European Telecommunications Standards Institute (ETSI), and Ministry of Telecommunications (MKK). The following sections provide an overview of the specifications for each type of PHY layer.

6.6.1.1 PMD Incorporating Universal Frequency Translation Technology

In the PHY layers of embodiments of the present invention, the PMD sublayer 12808 incorporates universal frequency translation technology to provide for frequency translation of transmitted and received WLAN communication signals. Universal frequency translation technology may be incorporated in transmitters, receivers, and transceivers in PMD sublayer 12808. As shown in FIG. 128B, PMD sublayer 12808 comprises one or more UFT modules 12810 in an embodiment. UFT module 12810 may be configured to provide for signal frequency up-conversion or down-conversion. One or more UFT modules 12810 may provide for carrier signal modulation with an information signal, and/or de-modulation, according a variety of modulation schemes. These modulation schemes include but are not limited to amplitude modulation (AM), frequency modulation (FM), or phase modulation (PM), including ASK, FSK, GFSK (Gaussian frequency shift keying), PSK, and DBPSK (differential binary phase shift keying), and combinations thereof. PMD sublayer 12808 may comprise one or more UFT modules for frequency translation of one or more signals. For example, two or more UFT modules may be configured to provide for, or assist in, I/Q modulation or demodulation of signals according to a variety of I/Q modulation schemes, including quadrature amplitude modulation (QAM), differential quadrature phase shift keying (DQPSK), quadrature phase shift keying (QPSK), complementary code keying (CCK), and packet binary convolutional coding (PBCC) modulation schemes. Systems and methods for handling these modulation schemes are further described herein. The UFT module of the present invention may be configured to accommodate further modulation schemes described elsewhere herein or otherwise known to persons skilled in the relevant art(s).

As shown in FIG. 128C, PMD sublayer 12808 may include one or more UFU modules 12812. UFU module 12812 comprises at least one UFT module 12810. Numerous embodiments for frequency up-converting and/or modulating signals via UFU module 12812 in PMD sublayer 12808 will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention.

As shown in FIG. 128C, PMD sublayer 12808 may include one or more UFD modules 12814. UFD module 12814 comprises at least one UFT module 12816. Numerous embodiments for frequency down-converting and/or demodulating signals via UFD module 12814 in PMD sublayer 12808 will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention.

As shown in FIG. 128D, PMD sublayer 12808 includes one or more UFU modules 12812 and one or more UFD modules 12814, which share one or more UFT modules 12812. UFU module 12812 and UFD module 12814 may share UFT module 12812, and/or share other components. Numerous embodiments for frequency up-converting signals and down-converting signals via UFU module 12812 and UFD module 12814 when sharing components will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention.

Frequency translation via universal frequency translation technology is described in further detail below, in regards to a variety of IEEE Std. 802.11 PHY layers.

6.6.2 Direct Sequence Spread Spectrum (DSSS) PHY

A DSSS PHY is one of the three PHY layers supported in the standard. The DSSS PHY uses the 2.4 GHz frequency band as the RF transmission media. Data transmission over the media is controlled by the DSSS PMD sublayer as directed by the DSSS PLCP sublayer. The DSSS PMD receives binary bits of information from the PLCP protocol data unit (PPDU) and transforms them into RF signals for the wireless media by using carrier modulation and DSSS techniques. FIG. 129A illustrates an exemplary DSSS PMD transmitter 12900. FIG. 129B illustrates an exemplary DSSS PMD receiver 12902. The DSSS PHY of the present invention may incorporate universal frequency translation technology for WLAN signal up-conversion, down-conversion, modulation, and de-modulation, as described in subsequent sub-sections.

6.6.2.1 DSSS PLCP Sublayer

A PLCP protocol data unit (PPDU) is unique to the DSSS PHY layer. FIG. 130 illustrates a PPDU frame 13002. PPDU frame 13002 includes a PLCP preamble 13004, PLCP header 13006, and MAC protocol data unit (MPDU) 13008. The receiver 12902 uses the PLCP preamble 13004 to acquire the incoming signal and synchronize the demodulator. The PLCP header 13006 includes information about the MPDU 13008 from the sending DSSS PHY. The PLCP preamble 13004 and PLCP header 13006 are typically transmitted at 1 Mbps, and the MPDU 13008 can be sent at 1 Mbps or 2 Mbps. The segments of the PPDU frame 13002 illustrated in FIG. 130 are described below:

SYNC: This field is 128 bits (symbols) in length and contains a string of 1's which are scrambled prior to transmission. The receiver uses this field to acquire the incoming signal and synchronize the receiver's carrier tracking and timing prior to receiving the start of frame delimiter (SFD).

Start of frame delimiter (SFD): This field contains information marking the start of a PPDU frame. The SFD specified is common for all IEEE 802.11 DSSS radios and uses the following hexadecimal word: F3A0hex.

Signal: The signal field defines which type of modulation must be used to receive the incoming MPDU. The binary value in this field is equal to the data rate multiplied by 100 kbit/s. In the June 1997 version of IEEE 802.11, two rates are supported: OAh for 1 Mbps DBPSK, and 14hex for 2 Mbps DQPSK.

Service: The service field is reserved for future use. The default value is 00h.

Length: The length field is an unsigned 16-bit integer that indicates the number of microseconds necessary to transmit the MPDU. The MAC layer uses this field to determine the end of a PPDU frame.

CRC: The CRC field contains the results of a calculated frame check sequence from the sending station. The calculation is performed prior to data scrambling. The CCITT CRC-16 error detection algorithm is used to protect the signal, service and length fields. The CRC-16 algorithm

is represented by the following polynomial: $G(x) = x^{16} + x^{12} + x^5 + 1$. The receiver performs the calculation on the incoming signal, service, and length fields and compares the results against the transmitted value. If an error is detected, the receiver's MAC makes the decision whether incoming PPDU should be terminated.

Embedded at the end of the MPDU portion of the PPDU is a field called FCS. This field contains a 32-bit CRC, which protects the information in the PLCP service data unit (PSDU). The DSSS PHY does not determine whether errors are present in the MPDU. The MAC makes that determination in a manner similar to the method used by the PHY layer.

6.6.2.2 Data Scrambling

Information bits transmitted by the DSSS PMD may be scrambled using a self-synchronizing 7-bit polynomial. The scrambling polynomial for the DSSS PHY may be: $G(z) = z^{-7} + z^{-4} + 1$. Scrambling is used to randomize the data in the SYNC field of the PLCP and data patterns which contain long strings of binary 1s or 0s. The receiver can descramble the information bits without prior knowledge from the sending station.

6.6.2.3 DSSS Modulation

In the June 1997 version of IEEE 802.11, the DSSS PMD uses differential phase shift keying (DPSK) as the modulation to transmit the PPDU. Two types of DPSK are specified. The DSSS PMD transmits the PLCP preamble and PLCP header at 1 Mbps using differential binary phase shift keying (DBPSK). The MPDU is sent at either 1 Mbps DBPSK or 2 Mbps differential quadrature phase shift keying (DQPSK), depending upon the content in the signal field of the PLCP header.

DPSK is a modulation technique which uses a balanced in-phase/quadrature (I/Q) modulator to generate a RF carrier. The RF carrier is phase modulated with symbols mapped from the binary bits in the PPDU. The symbols contain PPDU information. At the receiving station, data recovery

for DPSK is based on the phase differences between two consecutive symbols from the sending station. DPSK is non-coherent, meaning that a clock reference is not needed to recover the data. For 1 Mbps DBPSK, 1 and 0 binary bits in the PPDU constitute phase shifts of 180 degrees and the signal information is contained on the I-phase arm, as shown in constellation pattern 13102 of FIG. 131. For 2 Mbps DQPSK, two binary bits are combined from the PPDU, generating the following I/Q symbol pairs (00, 01, 11, 10). The phase shifts occur at 90 degrees for DQPSK, as shown in constellation pattern 13104 in FIG. 131. DQPSK is substantially similar to transmitting two 1 Mbps DBPSK signals, one on the I-phase, the other on the Q-phase. DBPSK is more tolerant to intersymbol interference caused by noise and multipath over the media; therefore DBPSK is generally used for the PLCP preamble.

For IEEE 802.11-compliant DSSS products, the rotation of DBPSK and DQPSK modulated symbols spinning about the I/Q constellation is counterclockwise. This is noteworthy because it is common to develop DSSS WLAN products that rotate in the opposite direction. This rotation is illustrated in FIG. 131.

6.6.2.4 Barker Spreading Method

The DSSS PHY layer is one of the two 2.4 GHz RF PHY layers to choose from in the IEEE 802.11 standard. Direct Sequence is the spreading method used. An 11-bit Barker word may be used as the spreading sequence. Every station in an IEEE 802.11 network uses the same 11-bit sequence. A Barker word sequence is classified as a short sequence, and is known to have very good correlation properties.

Barker word (11-bits) +1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1

In a transmitter, the 11-bit Barker word may be applied to a modulo-2 adder (XOR function) together with each of the information bits in the (scrambled) PPDU, as shown in FIG. 132A. The PPDU is

clocked at the information rate, for example, 1 Mbps, and the 11-Barker word is clocked at 11 Mbps (the chipping clock rate). The XOR function combines the signals by performing a modulo-2 addition on each PPDU bit with each Barker word bit (sometimes referred to as a chip). The output of the modulo-2 adder is a signal with a data rate that is 10x higher than the information rate. The result in the frequency domain is a signal that is spread over a wider bandwidth than the information signal, at a reduced RF power level. FIG. 132B illustrates an exemplary transmitter baseband signal before spreading 13202. FIG. 132C illustrates an exemplary transmitter baseband signal after spreading. At the receiver, the DSSS signal is convolved with the 11-bit Barker word and correlated. The correlation operation recovers the PPDU information bits at the transmitted information rate, and the undesired interfering in-band signals are spread out-of-band. FIG. 132D illustrates an exemplary receiver baseband signal before correlation. FIG. 132E illustrates an exemplary receiver baseband signal after correlation. The spreading and despreading of narrowband to a wideband signal is commonly referred to as processing gain, and is measured in decibels (0). Processing gain is the ratio of the DSSS signal rate to the PPDU information rate. The FCC and MKK specify the minimum requirement for processing gain as 10 dB in North America and Japan.

The Barker word used in IEEE 802.11 is different from the spreading codes used in code division multiple access (CDMA) and global positioning system (GPS). CDMA and GPS use orthogonal spreading codes, which allow multiple users to operate on the same channel frequency. CDMA codes can have longer sequences and have richer correlation properties.

6.6.2.5 DSSS Operating Channels and Transmit Power Requirements

Each DSSS PHY channel occupies 22 MHZ of bandwidth, and the spectral shape of the channel represents a filtered SinX/X function, as shown in FIG. 133. The DS channel transmit mask in IEEE 802.11 specifies that spectral products be filtered to -30dBr from the center frequency and all other products be filtered to -50dBr. This allows for three non-interfering channels spaced 25 MHZ apart in the 2.4 GHz frequency band. For example, the channel arrangement for North

America is illustrated in FIG. 134. With this channel arrangement, a user can configure multiple DSSS networks to operate simultaneously in the same area.

In IEEE 802.11 fourteen center frequency channels are defined for operation across the 2.4 GHz frequency band (see Table 1). In North America, twelve channels are allowed, ranging from 2.412 GHz to 2.462 GHz. In most of Europe, thirteen channels are allowed, ranging from 2.412 GHz to 2.472 GHz. In Japan, one channel frequency is reserved at 2.483 Ghz.

Channel Number	Frequency GHz	North America	Europe	Spain	France	Japan-MKK
1	2.412	X	X			
2	2.417	X	X			
3	2.422	X	X			
4	2.427	X	X			
5	2.432	X	X			
6	2.437	X	X			
7	2.442	X	X			
8	2.447	X	X			
9	2.452	X	X			
10	2.457	X	X	X	X	
11	2.462	X	X	X	X	
12	2.467		X		X	
13	2.472		X		X	
14	2.483					X

Table 1

In addition to frequency and bandwidth allocations, transmit power is a key parameter that is regulated worldwide. The maximum allowable radiated emissions for the DSSS PHY varies from region to region, as illustrated in Table 2. The transmit power is directly related to the range that a particular IEEE 802.11 DSSS PHY implementation can achieve. 100 mW is the nominal RF transmit power level for many of the IEEE 802.11 DSSS PHY wireless products on the market today.

1000 mW	North America
100 mW	Europe
10 mW/MHZ	Japan

Table 2

6.6.2.6 DSSS PMD Incorporating Universal Frequency Translation Technology

In embodiments, the DSSS PMD may incorporate universal frequency translation technology to provide for modulation/de-modulation and frequency translation of WLAN station signals. For instance, the DSSS PMD may comprise one or more UFT modules, such as UFT module 12810 of FIG. 128B, that provide for these functions. Furthermore, the DSSS PMD may comprise one or more UFU modules such as UFU module 12812 of FIG. 128C, and/or one or more UFD modules such as UFD module 12814 of FIG. 128C, to provide for modulation/de-modulation and frequency translation of WLAN station signals. The DSSS PMD of the present invention, using techniques of universal frequency translation, transmits and receives signals modulated according to DBPSK and DQPSK modulation schemes. Further specifications for these transmitted and received signals are provided above.

Embodiments for DSSS PMD transmitters and receivers incorporating universal frequency translation technology are provided below. Alternate embodiments (including equivalents,

extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the DSSS PMD as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software, or any combination thereof. The invention is intended and adapted to include such alternate embodiments.

6.6.2.6.1 Transmit DSSS PMD Incorporating Universal Frequency Translation

As shown in FIG. 129A, transmit DSSS PMD 12900 comprises a scrambler 12904, a spreader 12906, a transmit mask filter 12908, a DPSK modulation transmitter 12910, and an antenna 12912. The structure and operation of transmit DSSS PMD 12900 will be further described as follows, and is further described elsewhere herein.

Scrambler 12904 receives a PPDU signal 12914. In embodiments, PPDU signal 12914 comprises one or more whole PPDU frames and/or portions of PPDU frames. For example, in DSSS PMD embodiments transmitting according to DBPSK modulation, PPDU signal 12914 may comprise a PLCP preamble, a PLCP header, and/or an MPDU. In DSSS PMD embodiments transmitting according to DQPSK modulation, PPDU signal 12914 may comprise an MPDU. In alternate embodiments, the DSSS PMD PLCP preamble, PLCP header, and MPDU may be modulated according to any of the modulation schemes described herein.

Scrambler 12904 scrambles the PPDU signal 12914, and outputs a scrambled PPDU signal 12916. The design and use of a scrambler 12904 is well known to those skilled in the relevant art(s). A suitable scrambler 12904 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Spreader 12906 receives scrambled PPDU signal 12916. Spreader 12906 spreads the frequency spectrum of scrambled PPDU signal 12916, and outputs spread signal 12920. Spreader 12906 as shown in FIG. 129A is implemented as a modulo -2 adder, but other implementations are within the scope of the present invention. The design and use of a spreader 12906 is well known to

those skilled in the relevant art(s). A suitable spreader 12906 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Transmit mask filter 12908 receives spread signal 12920. Transmit mask filter 12908 filters spread signal 12920, and outputs filtered signal 12922. The design and use of a transmit mask filter 12908 is well known to those skilled in the relevant art(s). A suitable transmit mask filter 12908 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

DPSK modulation transmitter 12910 receives filtered signal 12922. DPSK modulation transmitter 12910 modulates an oscillating signal with filtered signal 12922 according to DBPSK modulation or DQPSK modulation, and frequency up-converts filtered signal 12922. DPSK modulation transmitter 12910 outputs transmitted modulated signal 12924, which is transmitted by antenna 12912.

The transmit DSSS PMD 12900 of FIG. 129A may incorporate universal frequency translation technology to provide for modulation and frequency up-conversion of WLAN station signals. FIG. 129C illustrates an exemplary embodiment of the DPSK modulation transmitter 12910 of FIG. 129A. Transmitter 12910 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Transmitter 12910 of FIG. 129C comprises at least one UFT module 12810. UFT module 12810 provides for modulation and frequency up-conversion of WLAN station signals to be transmitted. As described above, transmit DSSS PMD 12900 transmits the PLCP preamble and PLCP header at 1 Mbps using DBPSK, and the MPDU is sent at either 1 Mbps DBPSK or at 2 Mbps DQPSK, depending on the content in the signal field of the PLCP header. Numerous embodiments for transmitter 12910 will be known to persons skilled in the relevant art(s) from the teachings

herein, and are within the scope of the invention. Embodiments for transmitter 12910 incorporating UFT module 12810 are further described below and elsewhere herein.

6.6.2.6.1.1 UFU Module Transmitter Embodiments for DBPSK Modulation

FIG. 129D illustrates in greater detail an exemplary embodiment of transmitter 12910 of FIG. 129A. Transmitter 12910 comprises a DBPSK modulator 12946, a UFU module 12812, and an optional amplifier 12948.

DBPSK modulator 12946 of transmitter 12910 receives a filtered signal 12922. DBPSK modulator 12946 modulates filtered signal 12922, according to differential binary phase shift keying (DBPSK) modulation. For example, DBPSK modulator 12946 may DBPSK modulate an oscillating signal using filtered signal 12922. DBPSK modulation is well known to persons skilled in the relevant art(s). DBPSK modulator 12946 outputs modulated signal 12950. The design and use of a DBPSK modulator 12946 is well known to those skilled in the relevant art(s). A suitable DBPSK modulator 12946 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Modulated signal 12950 is received by UFU module 12812. UFU module 12812 includes at least one UFT module 12810. UFU module 12812 frequency up-converts modulated signal 12950, and outputs UFU module output signal 12952. Various structures and methods for operation of UFU module 12812 are described more fully elsewhere herein. The following subsection provides a structural and operational description of an embodiment of UFU module 12812.

When present, optional amplifier 12948 amplifies UFU module output signal 12952, outputting transmitted modulated signal 12924. Transmitted modulated signal 12924 comprises a DBPSK modulated signal.

Phase modulation techniques and other modulation techniques are more fully described in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998, the full disclosure of which is incorporated herein by reference in its entirety.

6.6.2.6.1.1.1 Detailed UFU Module Embodiment

FIG. 129E illustrates a more detailed exemplary circuit diagram of an embodiment of UFU module 12812. UFU module 12812 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

UFU module 12812 comprises a pulse-shaping circuit 12954, a first reference potential 12956, a filter 12958, a second reference potential 12960, a resistor 12962, and a UFT module 12810.

In FIG. 129E, pulse shaping circuit 12954 receives modulated signal 12950. Pulse shaping circuit 12954 outputs control signal 12964, which is preferably comprised of a string of pulses. Control signal 12964 controls UFT module 12810, which preferably comprises a switch. Various embodiments for UFT module 12810 are described above. One terminal of UFT module 12810 is coupled to a first reference potential 12960. The second terminal of UFT module 12810 is coupled through resistor 12962 to a second reference potential 12956. In a PM or PSK modulation embodiment, second reference potential 12956 is preferably a constant voltage level.

The output of UFT module 12810 is a harmonically rich signal 12966. Harmonically rich signal 12966 has a fundamental frequency and phase substantially proportional to control signal 12964, and an amplitude substantially proportional to the amplitude of second reference potential 12956. Each of the harmonics of harmonically rich signal 12966 also have phase proportional to

control signal 12964, and in a PM or PSK embodiment are thus considered to be PM or PSK modulated.

Harmonically rich signal 12966 is received by filter 12958. Filter 12958 preferably has a high Q. Filter 12958 preferably selects the harmonic of harmonically rich signal 12966 that is at the approximate frequency desired for transmission. Filter 12958 removes the undesired frequencies that exist as harmonic components of harmonically rich signal 12966. Filter 12958 outputs UFU module output signal 12952.

Further details pertaining to UFU module 12812 are provided in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998, which is incorporated herein by reference in its entirety.

Docket No. 1744.0630002

6.6.2.6.1.2 DBPSK Balanced Modulator Transmitter Embodiments

Balanced modulator transmitter configurations are presented in Section 3.1. These transmitter configurations may be applied in transmitter 12910 to modulate and frequency up-convert WLAN station signals according to DBPSK modulation techniques. The balanced modulator transmitter configurations presented above and applicable to transmitter 12910 include transmitter 7102 of FIG. 71A, transmitter 7162 of FIG. 71D, transmitter 7302 of FIG. 73A, and transmitter 7900 of FIG. 79A. Refer to Section 3.1 above for detailed description of these transmitters. Further details pertaining to balanced modulator transmitters are provided in co-pending U.S. Patent Application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Serial No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. 129F illustrates balanced modulator embodiments for transmitter 12910, according to the present invention. Transmitter 12910 comprises a DBPSK modulator 12968 and a transmitter 7102, 7162, 7302, 7900. The design and use of a DBPSK modulator 12968 is well known to those skilled in the relevant art(s). A suitable DBPSK modulator 12968 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

DBPSK modulator 12968 receives filtered signal 12922. DBPSK modulator 12968 produces an oscillating signal modulated with filtered signal 12922 according to DBPSK modulation. DBPSK modulator 12968 outputs DBPSK modulated signal 12970.

Transmitter 7102, 7162, 7302, 7900 receives DBPSK modulated signal 12970. DBPSK modulated signal 12970 of FIG. 129F corresponds to baseband signal 7110 of FIGS. 71A and 71D, baseband signal 7306 of FIG. 73A, and baseband signal 7902 of FIG. 79A. Transmitter 7102, 7162, 7302, 7900 may be one of transmitter 7102 of FIG. 71A, transmitter 7162 of FIG. 71D, transmitter 7302 of FIG. 73A, and transmitter 7900 of FIG. 79A, and other balanced modulator transmitter of the present invention described herein. The one of transmitters 7102, 7162, 7302, 7900 selected for a particular implementation of transmitter 12910 will depend on the particular application. Transmitter 7102, 7162, 7302, 7900 frequency up-converts DBPSK modulated signal 12970, and outputs transmitted modulated signal 12924. Transmitted modulated signal 12924 of FIG. 129F corresponds to output signal 7140 of FIGS. 71A and 71D, output signal 7322 of FIG. 73A, and output signal 7936 of FIG. 79A. Transmitted modulated signal 12924 comprises a DBPSK modulated information signal.

6.6.2.6.1.3 DQPSK Modulation Mode Transmitter Embodiments

Quadrature Phase-Shift Keying (QPSK) is a well known I/Q modulation technique for modulating digital signals using four phase states to code two digital bits per phase shift. An in-phase signal ("I") is modulated such that its phase varies as a function of one of the information signals, and a quadrature-phase signal ("Q") is modulated such that its phase varies as a function of the other information signal. The two modulated signals are combined to form an "QPSK" modulated signal and transmitted. In this manner, for instance, two separate information signals could be transmitted in a single signal simultaneously.

Embodiments are provided below for implementing QPSK transmitters and receivers that may be implemented in WLAN stations, according to embodiment of the present invention. For example, the QPSK transmitters described below may be implemented in transmit DSSS PMD sublayer 12900 to transmit DQPSK modulated WLAN signals. These transmitter embodiments are described herein for purposes of illustration, and not limitation. Alternate transmitter embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

In FIG. 129G, a QPSK modulation mode embodiment is presented. In this embodiment, two information signals are accepted. An in-phase signal ("I") is modulated such that its phase varies as a function of one of the information signals, and a quadrature-phase signal ("Q") is modulated such that its phase varies as a function of the other information signal. The two modulated signals are combined to form an "I/Q" modulated signal and transmitted. In this manner, for instance, two separate information signals could be transmitted in a single signal simultaneously. Other uses for this type of modulation would be apparent to persons skilled in the relevant art(s).

FIG. 129G illustrates an exemplary block diagram of a transmitter 12910 operating in an I/Q modulation mode. Transmitter 12910 comprises a signal separator 12972 and a QPSK modulation transmitter 12978.

Signal separator 12972 separates filtered signal 12922 into two signals: first information signal 12974 and second information signal 12976. When filtered signal 12922 is a bused signal, signal separator 12972 may merely be a location on the bus where filtered signal 12922 is separated into separate buses or data signals, for instance. Signal separator 12972 may alternatively comprise logic and memory for receiving and storing filtered signal 12922, and logically dividing it into the two signals. A suitable signal separator 12972 may be designed and implemented in software, firmware, hardware, and any combination thereof.

QPSK modulation transmitter 12978 comprises at least one UFT module 12810. QPSK modulation transmitter 12978 provides QPSK modulation to first information signal 12974 and second information signal 12976, outputting transmitted modulated signal 12924. Numerous embodiments for QPSK modulation transmitter 12978 will be recognized by persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Various embodiments for QPSK modulation transmitter 12978 are provided in the following subsections.

6.6.2.6.1.3.1 QPSK Modulation Transmitter Using Two UFU Modules

FIG. 129H illustrates a more detailed circuit block diagram for QPSK modulation transmitter 12978. QPSK modulation transmitter 12978 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

QPSK modulation transmitter 12978 comprises a first UFU module 12982, a second UFU module 12984, an oscillator 12988, a phase shifter 12990, a summer 12992, a first UFT module 12986, a second UFT module 12973, a first DBPSK modulator 12909, a second DBPSK modulator 12980, and a filter 12994.

Oscillator 12988 generates an "I"-oscillating signal 12996.

A first information signal 12974 is input to first DBPSK modulator 12909. The "I"-oscillating signal 12996 is modulated by first information signal 12974 in the first DBPSK modulator 12909, thereby producing an "I"-modulated signal 12901.

First UFU module 12982 inputs "I"-modulated signal 12901, and generates a harmonically rich "I" signal 12903 with a continuous and periodic wave form.

The phase of "I"-oscillating signal 12996 is shifted by phase shifter 12990 to create "Q"-oscillating signal 12998. Phase shifter 12990 preferably shifts the phase of "I"-oscillating signal 12996 by 90 degrees.

A second information signal 12976 is input to second DBPSK modulator 12980. "Q"-oscillating signal 12998 is modulated by second information signal 12976 in second DBPSK modulator 12980, thereby producing a "Q" modulated signal. The design and use of a first and second DBPSK modulator 12909 and 12980 is well known to those skilled in the relevant art(s). A suitable first and second DBPSK modulator 12909 and 12980 may be designed and implemented in software, firmware, hardware, and any combination thereof, or may be purchased "off the shelf."

Second UFU module 12984 inputs "Q" modulated signal 12975, and generates a harmonically rich "Q" signal 12905, with a continuous and periodic waveform.

Harmonically rich "I" signal 12903 and harmonically rich "Q" signal 12905 are preferably rectangular waves, such as square waves or pulses (although the invention is not limited to this embodiment), and are comprised of pluralities of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveforms. These sinusoidal waves are referred to as the harmonics of the underlying waveforms, and a Fourier analysis will determine the amplitude of each harmonic.

Harmonically rich "I" signal 12903 and harmonically rich "Q" signal 12905 are combined by summer 12992 to create harmonically rich "I/Q" signal 12907. Summers are well known to persons skilled in the relevant art(s).

Filter 12994 filters out the undesired harmonic frequencies, and outputs an transmitted modulated signal 12924 at the desired harmonic frequency or frequencies.

It will be apparent to persons skilled in the relevant art(s) that an alternative embodiment exists wherein the harmonically rich "I" signal 12903 and the harmonically rich "Q" signal 12905 may be filtered before they are summed, and further, another alternative embodiment exists wherein "I"-modulated signal 12901 and "Q"-modulated signal 12975 may be summed to create a QPSK-modulated signal before being routed to a switch module. Other QPSK modulation embodiments

will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention. Further details pertaining to an I/Q modulation mode transmitter are provided in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998, which is incorporated herein by reference in its entirety.

6.6.2.6.1.3.2 QPSK Modulation Transmitter Using Balanced Modulator

I/Q balanced modulator transmitter configurations are presented in Section 3.2. These transmitter configurations may be applied in transmitter 12910 to modulate and frequency up-convert WLAN station signals according to DQPSK modulation techniques. The I/Q balanced modulator transmitter configurations presented above and applicable to transmitter 12910 include I/Q transmitter 7420 of FIG. 74, I/Q transmitter 7608 of FIG. 76A, I/Q transmitter 7618 of FIG. 76B, I/Q transmitter 7702 of FIG. 77, I/Q transmitter 7802 of FIG. 78, I/Q transmitter 8000 of FIG. 80, I/Q transmitter 8200 of FIG. 82, and I/Q transmitter 8300 of FIG. 83. Refer to Section 3.2 above for detailed description of these transmitters. Further details pertaining to I/Q balanced modulator transmitters are provided in co-pending U.S. Patent Application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Serial No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. 129I illustrates I/Q balanced modulator embodiments for QPSK modulation transmitter 12978, according to the present invention. QPSK modulation transmitter 12978 comprises a first DBPSK modulator 12911, a second DBPSK modulator 12913, a pulse generator 7144, and an I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300. Further I/Q balanced modulator embodiments for QPSK modulation transmitter 12978 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

First DBPSK modulator 12911 receives I phase information signal 12974. First DBPSK modulator 12911 produces an oscillating signal modulated with I phase information signal 12976

according to DBPSK modulation. First DBPSK modulator 12911 outputs first DBPSK modulated signal 12977.

Second DBPSK modulator 12913 receives Q phase information signal 12976. Second DBPSK modulator 12913 produces an oscillating signal modulated with Q phase information signal 12976 according to DBPSK modulation. Second DBPSK modulator 12913 outputs second DBPSK modulated signal 12979. The design and use of a first and second DBPSK modulator 12911 and 12913 is well known to those skilled in the relevant art(s). Suitable first and second DBPSK modulators 12911 and 12913 may be designed and implemented in software, firmware, hardware, and any combination thereof, or may be purchased "off the shelf."

Pulse generator 7144 generates control signals 7123 and 7127 as described elsewhere herein.

I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300 receives first DBPSK modulated signal 12977, second DBPSK modulated signal 12979, and control signals 7123 and 7127. First DBPSK modulated signal 12977 of FIG. 129I corresponds to I baseband signal 7402 of FIGS. 74, 76A, 76B, 77, and 78, and I baseband signal 8002 of FIGS. 80, 82, and 83. I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300 may be one of I/Q transmitter 7420 of FIG. 74, I/Q transmitter 7608 of FIG. 76A, I/Q transmitter 7618 of FIG. 76B, I/Q transmitter 7702 of FIG. 77, I/Q transmitter 7802 of FIG. 78, I/Q transmitter 8000 of FIG. 80, I/Q transmitter 8200 of FIG. 82, and I/Q transmitter 8300 of FIG. 83, and other I/Q balanced modulator transmitter of the present invention described herein. The one of I/Q transmitters 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300 selected for a particular implementation of transmitter 12910 will depend on the particular application. I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300 combines and frequency up-converts first and second DBPSK modulated signals 12977 and 12979, and outputs transmitted modulated signal 12924. Transmitted modulated signal 12924 of FIG. 129I corresponds to output signal 7148 of FIGS. 74, 76A, 76B, 77, and 78, and output signal 8016 of FIGS. 80, 82, and 83. Transmitted modulated signal 12924 comprises a DQPSK modulated information signal.

6.6.2.6.2 Receiver DSSS PMD Incorporating Universal Frequency Translation

As shown in FIG. 129B, receiver DSSS PMD 12902 comprises an antenna 12926, a de-spread correlator 12928, a DPSK modulation receiver 12930, a de-scrambler 12932, a timing clock recovery module 12934. The structure and operation of receiver DSSS PMD 12902 will be further described as follows, and is further described elsewhere herein.

Antenna 12926 receives a transmitted modulated signal 12924. Transmitted modulated signal 12924 comprises an RF carrier signal modulated with an information signal according to DBPSK and/or DQPSK modulation techniques.

De-spread correlator 12928 receives transmitted modulated signal 12924 from antenna 12926, and receives an 11-bit Barker word. De-spread correlator 12928 convolves the received signal with the 11-bit Barker word and correlates it, and outputs a de-spread signal 12938. The design and use of a conventional de-spread correlator 12928 is well known to those skilled in the relevant art(s). A suitable conventional de-spread correlator 12928 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

DPSK modulation receiver 12930 receives de-spread signal 12938. DPSK modulation receiver 12930 demodulates and down-converts de-spread signal 12938, and outputs demodulated signal 12940.

De-scrambler 12932 receives demodulated signal 12940. De-scrambler 12932 de-scrambles demodulated signal 12940, and outputs PPDU signal 12942. PPDU signal 12942 comprises one or more PPDU frames and/or PPDU frame portions, such as a PLCP preamble, PLCP header, and MPDU. The design and use of a de-scrambler 12932 is well known to those skilled in the relevant art(s). A suitable de-scrambler 12932 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Timing clock recovery module 12924 is coupled to de-spread correlator 12928 and/or DBPSK/DQPSK de-modulator 12930. Timing clock recovery module 12924 may be used to recover

clocking/timing information from the received signal. Timing clock recovery module 12924 may output a data clock signal 12944, and may pass clocking/timing information back to de-spread correlator 12928 and/or DPSK modulation receiver 12930. The design and use of a timing clock recovery module 12924 is well known to those skilled in the relevant art(s). A suitable scrambler 12924 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Alternate embodiments for receiver DSSS PMD 12902 will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the positions of DPSK modulation receiver 12930 and de-spread correlator 12928 may be reversed. FIG. 129L illustrates a receiver DSSS PMD 12915 wherein DPSK modulation receiver 12930 receives transmitted modulated signal 12924, demodulates and down-converts transmitted modulated signal 12924, and outputs a demodulated signal that is received by de-spread correlator 12928. De-spread correlator 12928 convolves the received demodulated signal with the 11-bit Barker word and correlates it, and outputs a de-spread signal to de-scrambler 12932. The invention is intended and adapted to include such alternate embodiments.

The receiver DSSS PMD 12902 of FIG. 129B may incorporate universal frequency translation technology to provide for demodulation and frequency down-conversion of received WLAN station signals. FIG. 129J illustrates an exemplary embodiment of the DPSK modulation receiver 12930 of FIG. 129B. Receiver 12930 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver 12930 of FIG. 129J comprises at least one UFT module 12810. UFT module 12810 provides for demodulation and frequency down-conversion of received WLAN station signals. As described above, receiver DSSS PMD 12902 demodulates the DBPSK-modulated PLCP preamble and PLCP header, and demodulates the DBPSK- or DQPSK-modulated MPDU. Numerous

embodiments for receiver 12930 will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for receiver 12930 incorporating UFT module 12810 are further described below and elsewhere herein.

In a further embodiment, de-spread correlator 12928 comprises a UFT module. The UFT module may be used to convolve the received signal with the 11-bit Barker word, by coding a control signal received by the UFT module with the 11-bit Barker word. FIG. 129K illustrates a further embodiment of the present invention, where de-spread correlator 12928 and receiver 12930 share a UFT module 12810, to unify convolution of the received signal and down-conversion/demodulation of the received signal. Alternate embodiments for receiver DSSS PMD 12902 will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

6.6.2.6.2.1 UFD Module Receiver Embodiments for DBPSK Demodulation

FIG. 129M illustrates an embodiment of the DPSK modulation receiver 12930 of FIG. 129B. DPSK modulation receiver 12930 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

DPSK modulation receiver 12930 comprises a UFD module 12814, an optional amplifier 12917, and an optional filter 12919. UFD module 12814 comprises at least one UFT module 12810.

UFD module 12814 inputs de-spread signal 12938. De-spread signal 12938 comprises an oscillating signal modulated by an information signal according to DBPSK modulation techniques. UFD module 12814 frequency down-converts and demodulates de-spread signal 12938 to UFD module output signal 12921.

UFD module output signal 12921 is optionally amplified by optional amplifier 12917 and optionally filtered by optional filter 12919, and a down-converted baseband signal 2516 results. The amplifying and filtering functions may instead be provided for in optional signal conditioning module 2504, when present.

Received signals of a variety of modulation types may be down-converted directly to a baseband signal by DPSK modulation receiver 12930 of FIG. 129B. These modulation types include, but are not limited to phase modulation (PM), phase shift keying (PSK) including DBPSK, amplitude modulation (AM), amplitude shift keying (ASK), and combinations thereof.

In embodiments, UFD module 12814 frequency down-converts de-spread signal 12938 to a baseband signal. In alternative embodiments, UFD module 12814 down-converts de-spread signal 12938 to an intermediate frequency.

FIG. 129N illustrates an alternative embodiment of DPSK modulation receiver 12930 comprising a UFD module 12814 that down-converts de-spread signal 12938 to an intermediate frequency. DPSK modulation receiver 12930 of FIG. 129N comprises an intermediate frequency (IF) down-converter 12923. IF down-converter 12923 may comprise a UFD module and/or a UFT module, or may comprise a conventional down-converter. In this embodiment, UFD module output signal 12921 is output by UFD module 12814 at an intermediate frequency. This is an offset frequency, not at baseband. IF down-converter 12923 inputs UFD module output signal 12921, and frequency down-converts it to baseband signal 12925.

Baseband signal 12925 is optionally amplified by optional amplifier 12917 and optionally filtered by optional filter 12919, and a demodulated signal 12940 results.

DPSK modulation receiver 12930 may further comprise a third stage IF down-converter, and subsequent IF down-converters, as would be required or preferred by some applications. It will be apparent to persons skilled in the relevant art(s) how to design and configure such further IF down-converters from the teachings contained herein. Such implementations are within the scope of the present invention.

6.6.2.6.2.1.1 Detailed UFD Module Block Diagram

FIG. 129O illustrates an embodiment of UFD module 12814 in greater detail. This embodiment is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

UFD module 12814 comprises a storage device 12931, an oscillator 12927, a pulse-shaping circuit 2806, a reference potential 2808, and a UFT module 12810. As described above, many embodiments exist for UFD module 12814. For instance, in embodiments, oscillator 12927, or both oscillator 12927 and pulse-shaping circuit 12929, may be external to UFD module 12814.

Oscillator 12927 outputs oscillating signal 12935, which is input by pulse-shaping circuit 12929. The output of pulse-shaping circuit 12929 is a control signal 12937, which preferably comprises a string of pulses. Pulse-shaping circuit 12929 controls the pulse width of control signal 12937.

In an embodiment where de-spread correlator 12928 comprises a UFT module, the string of pulses of the corresponding control signal are coded according to the 11 bit-Barker word.

In embodiments, UFT module 12810 comprises a switch. Other embodiments for UFT module 12810 are within the scope of the present invention, such as those described above. One terminal of UFT module 12810 is coupled to a de-spread signal 12938, and a second terminal of UFT module 12810 is coupled to a first terminal of storage device 12931. A second terminal of storage device 12931 is coupled to a reference potential 2808 such as a ground, or some other potential. In a preferred embodiment, storage device 12931 is a capacitor. In an embodiment, the switch contained within UFT module 12810 opens and closes as a function of control signal 12937. As a result of the opening and closing of this switch, a down-converted signal, referred to as UFD module output signal 12921, results. Additional details pertaining to UFD module 12814 are

contained in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998, which is incorporated herein by reference in its entirety.

6.6.2.6.2.2 DBPSK Single Channel Receiver Embodiments

Single channel balanced receiver configurations are presented in Section 2.2.3. These receiver configurations may be applied in receiver 12930 to demodulate and frequency down-convert WLAN station signals according to DBPSK demodulation techniques. The single channel balanced receiver configurations presented above and applicable to receiver 12930 include receiver 11900 of FIG. 119. Refer to Section 2.2 above for detailed description of these receivers. Further details pertaining to balanced modulator receivers are provided in co-pending U.S. Patent Application entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Serial No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. 129P illustrates a single channel balanced demodulator embodiment for receiver 12930, according to the present invention. Receiver 12930 comprises a single channel receiver 11900. Further single channel balanced demodulator embodiments for receiver 12930 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Receiver 11900 receives de-spread signal 12938. De-spread signal 12938 of FIG. 129P corresponds to input RF signal 11906 of FIG. 119. Receiver 11900 frequency down-converts and demodulates de-spread signal 12938, and outputs demodulated signal 12940. Demodulated signal 12940 of FIG. 129P corresponds to baseband output signal 11908 of FIG. 119. Demodulated signal 12940 comprises an information signal.

6.6.2.6.2.3 DQPSK Modulation Mode Receiver Embodiments

FIG. 129Q illustrates an exemplary DQPSK modulation mode embodiment of a DPSK modulation receiver 12930, according to the present invention. This DQPSK modulation mode embodiment is described herein for purposes of illustration, and not limitation. Alternate DQPSK modulation mode embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver 12930 comprises a QPSK modulation receiver 12939. QPSK modulation receiver 12939 down-converts and demodulates an input signal that is modulated according to QPSK modulation techniques. QPSK modulation receiver 12939 down-converts and demodulates a received input signal to two baseband information signals. QPSK modulation receiver 12939 comprises at least one UFT module 12810. QPSK modulation receiver 12939 provides for QPSK demodulation to de-spread signal 12938, outputting demodulated signal 12940. Numerous embodiments for QPSK modulation receiver 12939 will be recognized by persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Various embodiments for QPSK modulation receiver 12939 are provided in the following subsections.

6.6.2.6.2.3.1 QPSK Modulation Receiver Using Two UFD Modules

FIG. 129R illustrates a more detailed circuit block diagram for QPSK modulation receiver 12939. QPSK modulation receiver 12939 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based

on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver 12930 comprises an oscillator 12949, a first UFD module 12941, a second UFD module 12943, a first UFT module 12945, a second UFT module 12947, a phase shifter 12951, a first optional amplifier 12953, a first filter 12955, a second optional amplifier 12957, and a second filter 12959.

Oscillator 12949 provides an oscillating signal used by both first UFD module 12941 and second UFD module 12943 via the phase shifter 12951. Oscillator 12949 generates an "I" oscillating signal 12961.

"I" oscillating signal 12961 is input to first UFD module 12941. First UFD module 12941 comprises at least one UFT module 12945. In an embodiment, first UFD module 12941 is structured similarly to UFD module 12814 of FIG. 129O, with oscillator 12949 substituting for oscillator 12927, and "I" oscillating signal 12961 substituting for oscillating signal 12935. First UFD module 12941 frequency down-converts and demodulates de-spread signal 12938 to down-converted "I" signal 12965 according to "I" oscillating signal 12961. Down-converted "I" signal 12965 may be an information signal with two possible states or voltage levels (QPSK). In further embodiments, down-converted "I" signal 12965 may be an information signal with more than two possible states or voltage levels (QAM).

Phase shifter 12951 receives "I" oscillating signal 12961, and outputs "Q" oscillating signal 12963, which is a replica of "I" oscillating signal 12961 shifted preferably by 90°.

Second UFD module 12943 inputs "Q" oscillating signal 12963. Second UFD module 12943 comprises at least one UFT module 12947. In an embodiment, second UFD module 12943 is structured similarly to UFD module 12814 of FIG. 129O with "Q" oscillating signal 12963 substituting for oscillating signal 12935. Second UFD module 12943 frequency down-converts and demodulates de-spread signal 12938 to down-converted "Q" signal 12967 according to "Q" oscillating signal 12963. Down-converted "Q" signal 12967 may be an information signal with two

possible states or voltage levels (QPSK). In further embodiments, down-converted "Q" signal 12967 may be an information signal with more than two possible states or voltage levels (QAM).

Down-converted "I" signal 12965 is optionally amplified by first optional amplifier 12953 and optionally filtered by first optional filter 12955, and a first information output signal 12969 is output.

Down-converted "Q" signal 12967 is optionally amplified by second optional amplifier 12957 and optionally filtered by second optional filter 12959, and a second information output signal 12971 is output.

In the embodiment depicted in FIG. 129R, first information output signal 12969 and second information output signal 12971 comprise demodulated signal 12940 of FIG. 129Q.

Alternate configurations for QPSK modulation receiver 12939 will be apparent to persons skilled in the relevant art(s) from the teachings herein. For instance, an alternate embodiment exists wherein phase shifter 12951 is coupled between de-spread signal 12938 and UFD module 12943, instead of the configuration described above. This and other such QPSK modulation mode receiver embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

6.6.2.6.2.3.2 QPSK Modulation Receiver Using Balanced Demodulator

I/Q balanced demodulator receiver configurations are presented in Section 2.2. These receiver configurations may be applied in receiver 12930 to demodulate and frequency down-convert WLAN station signals according to DQPSK demodulation techniques. The I/Q balanced demodulator receiver configurations presented above and applicable to receiver 12930 includes I/Q modulation receiver 10300 of FIG. 103. Refer to Section 2.2 above for detailed description of this receiver. Further details pertaining to I/Q balanced demodulator receivers are provided in co-pending U.S. Patent Application entitled "DC Offset, Re-radiation, and I/Q Solutions Using

Universal Frequency Translation Technology," Serial No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. 129S illustrates I/Q balanced demodulator embodiments for QPSK modulation receiver 12939, according to the present invention. QPSK modulation receiver 12939 comprises a control signal generator 12981 and an I/Q modulation receiver 10300 of FIG. 103. Further I/Q balanced demodulator embodiments for QPSK modulation receiver 12939 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Control signal generator 12981 generates control signals 10390, 10392, 10394 and 10396 as described elsewhere herein. Control signal generator 12981 may comprise a variety of control signal/pulse generator configurations as described elsewhere herein, including control signal generator 10400 of FIG. 104.

I/Q modulation receiver 10300 receives de-spread signal 12938 and control signals 10390, 10392, 10394 and 10396. De-spread signal 12938 corresponds to I/Q modulated RF input signal 10382 of FIG. 103. I/Q modulation receiver 10300 demodulates and frequency down-converts de-spread signal 12938, and outputs I baseband output signal 10384 and Q baseband output signal 10386, which form demodulated signal 12940. Demodulated signal 12940 comprises I baseband output signal 10384 and Q baseband output signal 10386.

6.6.3 Frequency Hopping Spread Spectrum (FHSS) PHY

As with the DSSS PHY, the FHSS PHY is one of the three PHY layers supported in the standard and uses the 2.4 GHz spectrum as the transmission media. Data transmission over the media is controlled by the FHSS PMD sublayer as directed by the FHSS PLCP sublayer. The FHSS PMD takes the binary bits of information from the whitened PSDU and transforms them into RF signals for the wireless media by using carrier modulation and FHSS techniques. FIGS. 135A and 135B illustrate block diagrams showing basic elements of the FHSS PMD transmitter and receiver,

respectively. Details of each are expanded upon in the subsequent section. The FHSS PHY of the present invention may incorporate universal frequency translation technology for WLAN signal up-conversion, down-conversion, modulation, and de-modulation, as described in subsequent sub-sections.

6.6.3.1 FHSS PLCP Sublayer

The PLCP preamble 13602, PLCP header 13604, and PLCP service data unit (PSDU) 13606 make up the PLCP protocol data unit (PPDU) 13600, as shown in FIG. 136. The PLCP preamble 13602 and PLCP header 13604 are unique to the FHSS PHY. The PLCP preamble 13602 is used to acquire the incoming signal and synchronize the receiver's demodulator. The PLCP header 13604 contains information about PSDU 13600 from the sending FHSS PHY. The PLCP preamble 13602 and PLCP header 13604 are transmitted at 1 Mbps (the basic rate).

SYNC: This field contains a string of alternating 0s and 1s, and is used by the receiver to synchronize the receiver's packet timing and correct for frequency offsets.

SFD: This field contains information marking the start of a PSDU frame. A common SFD is specified for all IEEE 802.11 FHSS radios using the following bit pattern: 0000l100101111101. The left most bit is transmitted first.

PLW: This field specifies the length of the PSDU in octets and is used by the MAC to detect the end of a PPDU frame.

PLCP signaling field (PSF): The PSF identifies the data rate of the whitened PSDU 13606, ranging from 1 Mbps to 4.5 Mbps in increments of 0.5 Mbps. Refer to Table 3 for the PSF bits corresponding to various data rates. The PLCP preamble 13602 and header 13604 are transmitted at the basic rate, 1 Mbps. The optional data rate for the whitened PSDU 13606 is 2 Mbps.

Bits 1-3	Data Rates – Mbps
000	1.0
001	1.5
010	2.0
011	2.5
100	3.0
101	3.5
110	4.0
111	4.5

Table 3

Header check error: This field contains the results of a calculated frame check sequence from the sending station. The calculation is performed prior to data whitening. The CCITT CRC-16 error detection algorithm is used to protect the PSF and PLW fields. The CRC-16 algorithm is represented by the following polynomial: $G(x) = x^{16} + x^{12} + x^5 + 1$. The receiver performs the calculation on the incoming PSF and PLW fields, and compares the results against the transmitted field. If an error is detected, the receiver's MAC determines if the incoming PPDU 13600 should be terminated.

Embedded at the end of the PSDU portion of the PPDU 13606 is a field called FCS. This field contains a 32-bit CRC, which protects the information in the PSDU. The FHSS PHY does not determine if errors are present in the PSDU. The MAC makes that determination, similar to the method used by the PHY.

6.6.3.2 PSDU Data Whitening

Data whitening is applied to the PSDU before transmission to minimize DC bias on the data if long strings of 1s or 0s are contained in the PSDU. The PHY stuffs a special symbol every 4

octets of the PSDU in a PPDU frame. A 127-bit sequence generator using the polynomial $S(x) = x^7 + x^4 + 1$ and a 32/33 bias-suppression encoding algorithm are used to randomize and whiten the data.

6.6.3.3 FHSS Modulation

In the June 1997 version of IEEE 802.11, the FHSS PMD uses two-level Gaussian frequency shift key (GFSK) modulation to transmit the PSDU 13606 at the basic rate of 1 Mbps. The PLCP preamble 13602 and PLCP header 13604 are transmitted at 1 Mbps. However, four-level GFSK is an optional modulation method defined in the standard that enables the whitened PSDU 13606 to be transmitted at a higher rate. The value contained in the PSF field of the PLCP header 13604 is used to determine the data rate of the PSDU 13606.

GFSK is a modulation technique used by the FHSS PMD, which deviates (shifts) the frequency either side of the carrier hop frequency depending on whether the binary symbol from the PSDU is a 1 or 0. A bandwidth bit period (Bt) = 0.5 is used. The changes in the frequency represent symbols containing PSDU information. For two-level GFSK, a binary 1 represents the upper deviation frequency from the hopped carrier, and a binary 0 represents the lower deviation frequency. The deviation frequency shall be greater than 110 KHz for IEEE 802.11 FHSS radios. The carrier frequency deviation is given by:

Binary 1 = $F_c + f_d$	Carrier hopped frequency plus the upper deviated frequency
Binary 0 = $F_c - f_d$	Carrier hopped frequency minus the lower deviated frequency

Four-level GFSK is similar to two-level GFSK, and is used to achieve a data rate of 2 Mbps in the same occupied frequency bandwidth. The modulator combines two binary bits from the whitened PSDU 13606 and encodes them into symbol pairs (10, 11, 01, 00). The symbol pairs generate four frequency deviations from the hopped carrier frequency, two upper and two lower. The symbol pairs are transmitted at 1 Mbps, and for each bit sent, the resulting data rate is 2 Mbps.

6.6.3.4 FHSS Channel Hopping

A set of hop sequences is defined in IEEE 802.11 for use in the 2.4 GHz frequency band. Hop channels are evenly spaced across the band over a span of 83.5 MHZ. During the development of the IEEE 802.11, the hop sequences listed in the standard were pre-approved for operation in North America, Europe, and Japan. The required number of hop channels is dependent upon the geographic location. In North America and Europe (excluding Spain and France) the number of hop channels is 79. The number of hop channels for Spain is 23 and for France is 35. In Japan, the required number of hop channels is 23. The hopped center channels are spaced uniformly across the 2.4 GHz frequency band occupying a bandwidth of 1 MHZ. In North America and Europe (excluding Spain and France) the hopped channels operate from 2.402 GHz to 2.480 GHz. For Japan, the hopped channels operate from 2.473 GHz to 2.495 GHz. In Spain, the hopped channels operate from 2.447 GHz to 2.473 GHz. For France, the hopped channels operate from 2.448 GHz to 2.482 GHz. Channel 2 is the first hopped channel located at a center frequency of 2.402 GHz, and channel 95 is the last hopped frequency channel in the 2.4 GHz band centered at 2.495 GHz.

Channel hopping is controlled by the FHSS PMD. The FHSS PMD transmits the whitened PSDU 13606 by hopping from channel to channel in a pseudorandom fashion using one of the hopping sequences. The hop rate is set by the regulatory bodies in the country of operation. In the US, FHSS radios must hop a minimum of 2.5 hops per second for a minimum hop distance of 6 MHZ. This is in accordance with the rules specified by the FCC rules under Part 15.

The hopping sequences for IEEE 802.11 are grouped in hopping sets for worldwide operation: Set 1, Set 2, and Set 3. The sequences are selected when a FHSS BSS is configured for a WLAN. The hopping sets are designed to minimize interference between neighboring FHSS radios in a set. The following hop sets are valid IEEE 802.11 hopping sequence numbers.

Operation in North America and most of Europe:

Set 1: (0, 3, 6, 9, 12, 15, 18, 21, 24, 27, 30, 33, 36, 39,42, 45, 48, 51, 54, 57, 60, 63, 66, 69, 72, 75)

Set 2: (1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31, 34, 37, 40, 43, 46, 49, 52, 55, 58, 61, 64, 67, 70, 73, 76)

Set 3: (2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 53, 56, 59,62, 65, 68, 72, 74, 77)

Operation in Spain:

Set 1: (0, 3, 6, 9, 12, 15, 18, 21, 24)

Set 2: (1, 4, 7, 10, 13, 16, 19, 22, 25)

Set 3: (2, 5, 8, 11, 14, 17, 20, 23, 26)

Operation in France:

Set 1: (0, 3, 6, 9, 12, 15, 18, 21, 24, 27, 30)

Set 2: (1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31)

Set 3: (2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32)

Operation in Japan:

Set 1: (6, 9, 12, 15)

Set 2: (7, 10, 13, 16)

Set 3: (8, 11, 14, 17)

6.6.3.5 FHSS PMD Incorporating Universal Frequency Translation

In embodiments, the FHSS PMD may incorporate universal frequency translation technology to provide for modulation/de-modulation and frequency translation of WLAN station signals. For instance, the FHSS PMD may comprise one or more UFT modules, such as UFT module 12810 of FIG. 128B, that provide for these functions. Furthermore, the FHSS PMD may comprise one or more UFU modules such as UFU module 12812 of FIG. 128C, and/or one or more UFD modules such as UFD module 12814 of FIG. 128C, to provide for modulation/de-modulation and frequency translation of WLAN station signals. The FHSS PMD of the present invention, using techniques of universal frequency translation, transmits and receives signals modulated according to 2-level and 4-level GFSK modulation schemes. Further specifications for these transmitted and received signals are provided above.

Embodiments for FHSS PMD transmitters and receivers incorporating universal frequency translation technology are provided below. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the FHSS PMD as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software, or any combination thereof. The invention is intended and adapted to include such alternate embodiments.

6.6.3.5.1 Transmit FHSS PMD Incorporating Universal Frequency Translation

As shown in FIG. 129A, transmit FHSS PMD 13500 comprises a data whitener 13504, a symbol mapping module 13506, a transmit Gaussian shaping filter 13508, a GFSK modulation transmitter 13510, and an antenna 13512. The structure and operation of transmit FHSS PMD 13500 will be further described as follows, and is further described elsewhere herein.

Data whitener 13504 receives a PSDU signal 13514. In embodiments, PSDU signal 13514 may comprise one or more PSDU frames to be modulated according to 2-level or 4-level GFSK modulation. In alternate embodiments, transmit FHSS PMD 13500 may receive a signal comprising the PLCP preamble and/or PLCP header, which may be modulated according to 2-level GFSK modulation. Alternatively, the FHSS PMD PSDU frame, PLCP preamble, and PLCP header may be modulated according to any of the modulation schemes described herein.

Data whitener 13504 whitens the PSDU signal 13514, and outputs a whitened PSDU signal 13516. Data whitener 13504 is present in 1 Mbps embodiments when necessary. The design and use of a data whitener 13504 is well known to those skilled in the relevant art(s). A suitable data whitener 13504 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Symbol mapping module 13506 receives optionally whitened PSDU signal 13516. Symbol mapping module 13506 symbol maps whitened PSDU signal 13516, and outputs mapped signal 13518. The design and use of a symbol mapping module 13506 is well known to those skilled in the relevant art(s). A suitable symbol mapping module 13506 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Transmit Gaussian shaping filter 13508 receives mapped signal 13518. Transmit Gaussian shaping filter 13508 filters mapped signal 13518, and outputs filtered signal 13520. The design and use of a transmit Gaussian shaping filter 13508 is well known to those skilled in the relevant art(s). A suitable transmit Gaussian shaping filter 13508 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

GFSK modulation transmitter 13510 receives filtered signal 13520. GFSK modulation transmitter 13510 modulates an oscillating signal with filtered signal 13520 according to 2-level or 4-level GFSK, and frequency up-converts filtered signal 13520. GFSK modulation transmitter 13510 outputs transmitted modulated signal 13522, which is transmitted by antenna 13512.

The transmit FHSS PMD of FIG. 135A may incorporate universal frequency translation technology to provide for modulation and frequency up-conversion of WLAN station signals. FIG.

135C illustrates an exemplary embodiment of the GFSK modulation transmitter 13510 of FIG. 135A. Transmitter 13510 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Transmitter 13510 of FIG. 135C comprises at least one UFT module 12810. UFT module 12810 provides for modulation and frequency up-conversion of WLAN station signals to be transmitted. As described above, transmit FHSS PMD 13500 transmits the PLCP preamble and PLCP header at 1 Mbps using 2-level GFSK, and the PSDU is sent at either 1 Mbps 2-level GFSK or at 2 Mbps 4-level GFSK, depending on the content in the PSF field of the PLCP header. Numerous embodiments for transmitter 13510 will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for transmitter 13510 incorporating UFT module 12810 are further described below and elsewhere herein.

6.6.3.5.1.1 UFU Module Transmitter Embodiments for GFSK Modulation

FIG. 135D illustrates in greater detail an exemplary embodiment of transmitter 13510 of FIG. 135A. Transmitter 13510 comprises a GFSK modulator 13538, a UFU module 12812, and an optional amplifier 13540.

GFSK modulator 13538 of transmitter 13510 receives a filtered signal 13520. GFSK modulator 13538 modulates filtered signal 13520, according to Gaussian frequency shift keying (GFSK) modulation. For example, GFSK modulator 13538 may frequency modulate an oscillating signal using filtered signal 13520. GFSK modulator 13538 outputs modulated signal 13542. The design and use of a GFSK modulator 13538 is well known to those skilled in the relevant art(s). A

suitable GFSK modulator 13538 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Modulated signal 13542 is received by UFU module 12812. UFU module 12812 includes at least one UFT module 12810. UFU module 12812 frequency up-converts modulated signal 13542, and outputs UFU module output signal 13544. Various structures and methods for operation of UFU module 12812 are described more fully elsewhere herein. For example, Section 6.6.2.6.1.1.1 provides an exemplary structural and operational description of an embodiment of UFU module 12812 in FIG. 129E, where in the present GFSK embodiment, modulated signal 13542 is input to pulse shaping circuit 12954. Hence, each of the harmonics of harmonically rich signal 12966 have frequency proportional to control signal 12964, and in a GFSK embodiment are thus considered to be GFSK modulated.

When present, optional amplifier 13540 amplifies UFU module output signal 13544, outputting transmitted modulated signal 13522. Transmitted modulated signal 13522 comprises a GFSK modulated signal.

Further embodiments for up-converting FSK modulated signals are described in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998, the full disclosure of which is incorporated herein by reference in its entirety.

6.6.3.5.1.2 GFSK Balanced Modulator Transmitter Embodiments

Balanced modulator transmitter configurations are presented in Section 3.1. These transmitter configurations may be applied in transmitter 13510 of FIG. 135A to modulate and frequency up-convert WLAN station signals according to GFSK modulation techniques. The balanced modulator transmitter configurations presented above and applicable to transmitter 13510 include transmitter 7102 of FIG. 71A, transmitter 7162 of FIG. 71D, transmitter 7302 of FIG. 73A, and transmitter 7900 of FIG. 79A. Refer to Section 3.1 above for detailed description of these transmitters. Further details pertaining to balanced modulator transmitters are provided in co-

pending U.S. Patent Application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Serial No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. 135E illustrates balanced modulator embodiments for transmitter 13510, according to the present invention. Transmitter 13510 comprises a GFSK modulator 13546 and a transmitter 7102, 7162, 7302, 7900. Further balanced modulator embodiments for transmitter 13510 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

GFSK modulator 13546 receives filtered signal 13520. GFSK modulator 13546 produces an oscillating signal modulated with filtered signal 13520 according to GFSK modulation. GFSK modulator 13546 outputs GFSK modulated signal 13548. The design and use of a GFSK modulator 13546 is well known to those skilled in the relevant art(s). A suitable GFSK modulator 13546 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Transmitter 7102, 7162, 7302, 7900 receives GFSK modulated signal 13548. GFSK modulated signal 13548 of FIG. 135E corresponds to baseband signal 7110 of FIGS. 71A and 71D, baseband signal 7306 of FIG. 73A, and baseband signal 7902 of FIG. 79A. Transmitter 7102, 7162, 7302, 7900 may be one of transmitter 7102 of FIG. 71A, transmitter 7162 of FIG. 71D, transmitter 7302 of FIG. 73A, and transmitter 7900 of FIG. 79A, and other balanced modulator transmitter of the present invention described herein. The one of transmitters 7102, 7162, 7302, 7900 selected for a particular implementation of transmitter 13510 will depend on the particular application. Transmitter 7102, 7162, 7302, 7900 frequency up-converts GFSK modulated signal 13548, and outputs transmitted modulated signal 13522. Transmitted modulated signal 13522 of FIG. 135E corresponds to output signal 7140 of FIGS. 71A and 71D, output signal 7322 of FIG. 73A, and output signal 7936 of FIG. 79A. Transmitted modulated signal 13522 comprises a GFSK modulated information signal.

6.6.3.5.2 Receiver FHSS PMD Incorporating Universal Frequency Translation

As shown in FIG. 135B, receiver FHSS PMD 13502 comprises an antenna 13530, a GFSK modulation receiver 13524, a data de-whitener 13526, a hop timing recovery module 13528. The structure and operation of receiver FHSS PMD 13502 will be further described as follows, and is further described elsewhere herein.

Antenna 13530 receives a transmitted modulated signal 13522. Transmitted modulated signal 13522 comprises an RF carrier signal modulated with an information signal according to 2-level or 4-level GFSK modulation techniques.

GFSK modulation receiver 13524 receives transmitted modulated signal 13522 from antenna 13530. GFSK modulation receiver 13524 demodulates and down-converts transmitted modulated signal 13522, and outputs demodulated signal 13532. Demodulated signal 13532 comprises one or more PPDU frames and/or PPDU frame portions, such as a PLCP preamble, PLCP header, and PSDU.

Data de-whitener 13526 receives demodulated signal 13532. Data de-whitener 13526 de-whitens demodulated signal 13532, and outputs PSDU signal 13534. PSDU signal 13534 comprises one or more PSDU frames. Data de-whitener 13526 is present in 2-level GFSK embodiments when necessary. The design and use of a data de-whitener 13526 is well known to those skilled in the relevant art(s). A suitable data de-whitener 13526 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Hop timing recovery module 13528 is coupled to GFSK modulation receiver 13524. Hop timing recovery module 13528 may be used to recover hop timing/clocking information from the received signal. Hop timing recovery module 13528 may output a data clock signal 13536, and may pass hop timing/clocking information back to GFSK modulation receiver 13524. The design and use of a hop timing recovery module 13528 is well known to those skilled in the relevant art(s). A suitable hop timing recovery module 13528 may be designed and implemented in software, firmware, hardware, and any combination thereof.

Alternate embodiments for receiver FHSS PMD 13502 will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The receiver FHSS PMD 13502 of FIG. 135B may incorporate universal frequency translation technology to provide for demodulation and frequency down-conversion of received WLAN station signals. FIG. 135F illustrates an exemplary embodiment of the GFSK modulation receiver 13524. Receiver 13524 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver 13524 of FIG. 135F comprises at least one UFT module 12810. UFT module 12810 provides for demodulation and frequency down-conversion of received WLAN station signals. As described above, receiver FHSS PMD 13502 demodulates the 2-level GFSK-modulated PLCP preamble and PLCP header, and demodulates the 2-level or 4-level GFSK-modulated PSDU. Numerous embodiments for receiver 13524 will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for receiver 13524 incorporating UFT module 12810 are further described below and elsewhere herein.

6.6.3.5.2.1 UFD Module Receiver Embodiments for GFSK Demodulation

Various embodiments for receiver 13524 exist, where receiver 13524 comprises one or more UFD modules, and are described elsewhere herein. For instance, receiver 13524 may comprise a UFD module 12814, as shown in FIGS. 128C and 128D. These embodiments are adaptable to demodulation of GFSK modulated signals such as transmitted modulated signal 13522.

For example, Section 6.6.2.6.2.1 provides exemplary structural and operational description of embodiments comprising a UFD module 12814 for signal down-conversion and demodulation. The configurations shown in FIGS. 129M and 129N for receiver 12930 are adaptable to receiver 13524 for down-conversion of GFSK modulated WLAN signals. Receiver 135242 may be configured as shown for receiver 12930 in FIGS. 129M and 129N to down-convert and demodulate transmitted modulated signal 13522. As described above, transmitted modulated signal 13522 is modulated according to GFSK.

In the demodulator configurations of FIG. 129M and 129N, transmitted modulated signal 13522 is input to UFD module 12814. UFD module 12814 frequency down-converts and demodulates transmitted modulated signal 13522 to UFD module output signal 12921. In the embodiment shown in FIG. 129M, UFD module 12814 frequency down-converts transmitted modulated signal 13522 to a baseband signal. In the embodiment shown in FIG. 129N, UFD module 12814 down-converts transmitted modulated signal 13522 to an intermediate frequency. Demodulated signal 12940 of FIGS. 129M and 129N corresponds to demodulated signal 13532 of FIG. 135B. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Various structures and methods for operation of UFD module 12814 are described more fully elsewhere herein. For example, Section 6.6.2.6.2.1.1 provides an exemplary structural and operational description of an embodiment of UFD module 12814, shown in FIG. 129O, where in a GFSK embodiment, transmitted modulated signal 13522 is input to UFT module 12810.

6.6.3.5.2.2 GFSK Single Channel Receiver Embodiments

Single channel balanced receiver configurations are presented in Section 2.2.3. These receiver configurations may be applied in receiver 13524 to demodulate and frequency down-convert

WLAN station signals according to GFSK demodulation techniques. The single channel balanced receiver configurations presented above and applicable to receiver 13524 include receiver 11900 of FIG. 119. Refer to Section 2.2 above for detailed description of these receivers. Further details pertaining to balanced modulator receivers are provided in co-pending U.S. Patent Application entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Serial No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. 135G illustrates a single channel balanced demodulator embodiment for receiver 13524, according to the present invention. Receiver 13524 comprises a single channel receiver 11900. Further single channel balanced demodulator embodiments for receiver 13524 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Receiver 11900 receives transmitted modulated signal 13522. Transmitted modulated signal 13522 of FIG. 135G corresponds to input RF signal 11906 of FIG. 119. Receiver 11900 frequency down-converts and demodulates transmitted modulated signal 13522, and outputs demodulated signal 13532. Demodulated signal 13532 of FIG. 135G corresponds to baseband output signal 11908 of FIG. 119. Demodulated signal 13532 comprises an information signal.

6.6.4 Infrared (IR) PHY

As stated previously, the infrared (IR) PHY is one of the three PHY layers supported in the IEEE 802.11 standard. The IR PHY differs from DSSS and FHSS in using near-visible light as the transmission media. IR communication relies on light energy, which may be reflected by objects and travels by line-of-sight. IR PHY operation is generally restricted to indoor environments. The IR PHY signal typically does not pass through walls, as can the DSSS and FHSS radio signals. Data transmission over the media is controlled by the IR PMD sublayer as directed by the IR PLCP sublayer. The IR PMD takes the binary bits of information from the PSDU and transforms them into light energy emissions for the wireless media by using carrier modulation. FIG. 137 illustrates a

block diagram of an exemplary IR PMD sublayer 13700. IR PMD sublayer 13700 comprises a transmitter 13702 and a receiver 13704. Further details of each are provided in subsequent sub-sections.

6.6.4.1 IR PLCP Sublayer

A PLCP preamble 13802, PLCP header 13804, and PSDU 13806 make up a PPDU 13600, as shown in FIG. 138. The PLCP preamble 13802 and PLCP header 13804 are unique to the IR PHY. The PLCP preamble 13802 is used to acquire the incoming signal and synchronize the receiver prior to the arrival of the PSDU 13806. The PLCP header 13804 contains information about the PSDU 13806 from the sending IR PHY. The PLCP preamble 13802 and PLCP header 13804 are transmitted at 1 Mbps, and the PSDU 13806 can be sent at 1 Mbps or 2 Mbps.

SYNC: This field contains a sequence of alternating pulse presence and absence in consecutive time slots. The SYNC field is used by the IR PHY to perform signal acquisition and clock recovery. The standard specifies 57 time slots as the minimum and 73 time slots as the maximum.

SFD: This field contains information that marks the start of a PPDU frame. A common SFD is specified for all IEEE 802.11 IR implementations. The SFD is represented by the following bit pattern: 1001

Data rate: This field defines the data rate at which the PPDU 13600 is transmitted. There are two rates to choose from: 000 corresponding to 1 Mbps (the basic rate), and 001 corresponding to 2 Mbps (the enhanced access rate). The PLCP preamble 13802 and PLCP header 13804 are sent at the basic rate 1 Mbps.

DC level: This field contains information that allows the IR PHY to stabilize the DC level after receiving the preamble and data rate fields. The supported data rates use the following bit patterns:

1 Mbps: 00000000100000000000000010000000

2 Mbps: 00100010001000100010001000100010

Length: This field contains an unsigned 16-bit integer that indicates the number of microseconds to transmit the PSDU 13806. The MAC layer may use this field to detect the end of a frame.

Frame check sequence: This field contains the calculated 16-bit CRC result from the sending station. The CCITT CRC-16 error detection algorithm is used to protect the length field. The CRC-16 algorithm is represented by the following polynomial: $G(x) = x^{16} + x^{12} + x^5 + 1$. The receiver performs the calculation on the incoming Length field and compares the results against the transmitted field. If an error is detected, the receiver's MAC determines whether the incoming PSDU 13806 should be terminated.

Embedded at the end of the PSDU 13806 of the PPDU 13600 is a field called FCS. This field contains a 32-bit CRC, which is used to protect the information in the PSDU 13806. The IR PHY does not determine whether errors are present in the PSDU 13806. The MAC makes this determination in a manner similar to that used by the PHY layer.

6.6.4.2 IR PHY Modulation Method

The IR PHY transmits binary data at 1 and 2 Mbps using a modulation scheme known as pulse position modulation (PPM). PPM is used in IR systems to reduce the optical power required to be provided by the LED infrared source. The specific data rate is dependent upon the type of PPM. The modulation for 1 Mbps operation is 16-PPM. The modulation for 2 Mbps is 4-PPM. PPM keeps the amplitude and pulse width constant, and varies the position of the pulse in time. Each pulse position represents a different symbol in time.

For 16-PPM, each group of data bits of the PSDU is mapped to one of the 16-PPM symbols for 1 Mbps operation. Notice in Table 4 a "1" bit in the 16-PPM symbol represents data bit position.

The order of bit transmission is left to right. The data bits are arranged (gray coded) to reduce the possibility of multiple bit errors due to intersymbol interference in the media.

Data Bits	16-PPM Symbols
0000	0000000000000001
0001	0000000000000010
0011	0000000000000100
0010	0000000000001000
0110	0000000000010000
0111	0000000000100000
0101	0000000001000000
0100	0000000010000000
1100	0000000100000000
1101	0000001000000000
1111	0000010000000000
1110	0000100000000000
1010	0001000000000000
1011	0010000000000000
1001	0100000000000000
1000	1000000000000000

Table 4

For 4-PPM, two data bits are paired in the PSDU to form a 4-bit symbol map as shown in Table 5. The order of bit transmission is left to right.

Data Bits	4-PPM Symbol
00	0001
01	0010
11	0100
10	1000

Table 5

6.6.5 Geographic Regulatory Bodies

WLAN IEEE 802.11-compliant DSSS and FHSS radios operating in the 2.4 GHz frequency band must comply with local geographical regulatory domains before operating in this spectrum. These products are subject to certification. The technical requirements in the IEEE 802.11 standard were developed to comply with the regulatory agencies of North America, Europe, and Japan. The regulatory agencies in these regions set emission requirements for WLANs to minimize the amount of interference a radio can generate or receive from another in the same proximity. The regulatory requirements do not affect the interoperability of IEEE 802.11-compliant products. It is the responsibility of product developers to investigate and comply with the regulatory agencies. In some situations, additional certifications are necessary for regions within Europe, or outside of Japan or North America. Listed below are agencies defined by IEEE 802.11.

6.6.5.1 North America

Approval Standards: Industry Canada

Documents: GL36

Approval Authorities: Federal Communications Commission, (FCC)

USA Documents: CFR 47, Part 15 Sections 15.205, 15.209, 15.247

Approval Authority: Industry Canada, FCC (USA)

6.6.5.2 Spain

Approval Standards: Supplemento Del Numero 164 Del Boletin Oficial Del Estado (Published 10, July 91, Revised 25 June 93)
Documents: ETS 300-328, ETS 300-339
Approval Authority: Cuadro Nacional De Atribucion De Frecuesias

6.6.5.3 Europe

Approval Standards: European Telecommunications Standards Institute
Documents: ETS 300-328, ETS 300-339
Approval Authority: National Type Approval Authorities

6.7 Physical Layer Extensions to IEEE 802.11

In October 1997, the IEEE 802 Executive Committee approved two projects for higher rate physical layer (PHY) extensions to the IEEE 802.11 standard. The first extension, IEEE 802.11a, defines requirements for a PHY operating in the 5.0 GHz U-NII frequency, with data rates ranging from 6 Mbps to 54 Mbps. The second extension, IEEE 802.11b, defines a set of PHY specifications operating in the 2.4 GHz ISM frequency band at rates up to 11 Mbps. Both PHY extensions are defined to operate with the existing MAC. The following sections provide further detail of the two extensions.

6.7.1 IEEE 802.11a -The OFDM Physical Layer

The IEEE 802.11a PHY is one of the physical layer (PHY) extensions of IEEE 802.11 and is referred to as the orthogonal frequency division multiplexing (OFDM) PHY. The OFDM PHY provides the capability to transmit PSDU frames at multiple data rates up to 54 Mbps for WLAN networks where transmission of multimedia content is a consideration. The OFDM PHY defined for IEEE 802.11a is similar to the OFDM PHY specification of ETSI-HIPERLAN (High Performance Radio Local Area Network) II. The OFDM PHY of the present invention may incorporate universal frequency translation technology for WLAN signal up-conversion, down-conversion, modulation, and de-modulation, as described in subsequent sub-sections.

In the OSI structure, the PHY's PLCP sublayer and PMD sublayer are unique to the OFDM PHY. The following sections provide further detail of the PLCP header, data rates, and modulations defined in IEEE 802.11a.

6.7.1.1 OFDM PLCP Sublayer

The PPDU 13900 is unique to the OFDM PHY. The PPDU 13900 consists of a PLCP preamble 13902, a signal field 13904, and a data field 13906, as shown in FIG. 139. The receiver uses the PLCP preamble 13902 to acquire the incoming OFDM signal and synchronize the demodulator. The PLCP header 13908 contains information about the PSDU 13910 from the sending OFDM PHY. The PLCP preamble 13902 and the signal field 13904 are transmitted at 6 Mbps, binary phase shift keying (BPSK)-OFDM modulated using convolutional encoding rate R = ½.

PLCP preamble: This field is used to acquire the incoming signal, and to train and synchronize the receiver. The PLCP preamble 13902 consists of twelve symbols, including ten short symbols and two long symbols. The short symbols are used to train the receiver's AGC, and to obtain a coarse estimate of the carrier frequency and the channel. The long symbols are used to fine-

tune the frequency and channel estimates. Twelve subcarriers are used for the short symbols and 53 for the long symbols. The training of an OFDM is accomplished in 16 μs. The PLCP preamble 13902 is BPSK-OFDM modulated at 6 Mbps.

Signal: The signal 13904 is a 24-bit field, which includes information about the rate and length of the PSDU 13910. The signal field 13904 is convolutional encoded rate ½, BPSK-OFDM modulated. Four bits (R1-R4) are used to encode the rate, eleven bits are defined for the length, one bit is reserved, one bit is a parity bit, and six bits form a "0" tail. The rate bits (R1-R4) are defined in Table 6. The mandatory data rates for IEEE 802.11a-compliant systems are 6 Mbps, 12 Mbps, and 24 Mbps.

Rate	Modulation	Coding Rate	Signal bits (R1-R4)
6 Mbps	BPSK	R = ½	1101
9 Mbps	BPSK	R = ¾	1111
12 Mbps	QPSK	R = ½	0101
18 Mbps	QPSK	R = ¾	0111
24 Mbps	16QAM	R = ½	1001
36 Mbps (optional)	16QAM	R = ¾	1011
48 Mbps (optional)	64QAM	R = 2/3	0001
54 Mbps (optional)	64QAM	R = ¾	0011

Table 6

Length: The length field includes an unsigned 12-bit integer that indicates the number of octets in the PSDU 13910.

Data: The data field contains the service field, the PSDU 13910, tails bits 13912, and pad bits 13914. A total of six tail bits containing 0s are appended to the PPDU 13900 to ensure that the convolutional encoder is brought back to a zero state. The equation for determining the number of bits in the data field 13906, the number of tail bits 13912, the number of OFDM symbols, and the number pad bits 13914 is defined in IEEE 802.11a. The data portion of the packet is transmitted at the data rate indicated in the signal field 13904.

6.7.1.2 Data Scrambler

Bits transmitted by the OFDM PMD in the data portion are scrambled using a frame-synchronous 127-bit sequence generator. The scrambling is used to randomize the service, PSDU 13910, pad bit 13914, and data patterns, which may contain long strings of binary 1s or 0s. The tail bits 13912 are not scrambled. The scrambling polynomial for the OFDM PHY is: $S(x) = x^{-7} + x^{-4} + 1$. The initial state of the scrambler is randomly chosen. Prior to scrambling the PPDU frame 13900, the seven least significant bits of the service field are reset to 0 in order to estimate the initial state of the scrambler in the receiver.

6.7.1.3 Convolutional Encoding

All information contained in the service field, PSDU 13910, tail field 13912, and pad field 13914 are encoded using a convolutional encoding rate R = ½, 2/3, or ¾ corresponding to the desired data rate. Convolutional encoding is generated using the following polynomials; $g_0 = 133_8$ and $g_1 = 171_8$ of rate R = ½. Puncture codes are used for the higher data rates. Industry standard algorithms, such as the Viterbi algorithm, are recommended for decoding.

6.7.1.4 OFDM Modulation

In July 1998, the IEEE 802.11 Working Group adopted OFDM modulation as the basis for IEEE 802.11a. This OFDM method is similar to the modulation technique adopted in Europe by the ETSI-HIPERLAN II 5 GHz radio PHY specification. The basic principal of operation first divides a high-speed binary signal to be transmitted into a number of lower data rate subcarriers. There are 48 data subcarriers and 4 carrier pilot subcarriers for a total of 52 nonzero subcarriers defined in IEEE 802.11a. Each lower data rate bit stream is used to modulate a separate subcarrier from one of the channels in the 5 GHz band. Intersymbol interference is generally not a concern for a lower speed carrier. However, the subchannels may be subjected to frequency selective fading. Therefore, bit interleaving and convolutional encoding is used to improve the bit error rate performance. The scheme uses integer multiples of the first subcarrier, which are orthogonal to each other. This technique is known as orthogonal frequency division multiplexing (OFDM). Prior to transmission, the PPDU is encoded using a convolutional coded rate R = ½, and the bits are reordered and bit interleaved for the desired data rate. Each bit is then mapped into a complex number according to the modulation type, and subdivided into 48 data subcarriers and 4 pilot subcarriers. The subcarriers are combined using an inverse fast Fourier transform (FFT) and transmitted. At the receiver, the carrier is converted back to a multi-carrier lower data rate form using an FFT. The lower data rate subcarriers are combined to form the high rate PPDU. Exemplary block diagrams of an IEEE 802.11a OFDM PMD transmitter and receiver are illustrated in FIGS. 140A and 140B, respectively.

6.7.1.5 OFDM PMD Incorporating Universal Frequency Translation Technology

In embodiments, the OFDM PMD may incorporate universal frequency translation technology to provide for modulation/de-modulation and frequency translation of WLAN station signals. For instance, the OFDM PMD may comprise one or more UFT modules, such as UFT module 12810 of FIG. 128B, that provide for these functions. Furthermore, the OFDM PMD may

comprise one or more UFU modules such as UFU module 12812 of FIG. 128C, and/or one or more UFD modules such as UFD module 12814 of FIG. 128C, to provide for modulation/de-modulation and frequency translation of WLAN station signals. The OFDM PMD of the present invention, using techniques of universal frequency translation, transmits and receives signals modulated according to BPSK, QPSK, 16-QAM, and 64-QAM modulation schemes. Further specifications for these transmitted and received signals are provided above.

Embodiments for OFDM PMD transmitters and receivers incorporating universal frequency translation technology are provided below. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the OFDM PMD as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software, or any combination thereof. The invention is intended and adapted to include such alternate embodiments.

6.7.1.5.1 Transmit OFDM PMD Incorporating Universal Frequency Translation

As shown in FIG. 129A, transmit OFDM PMD 14000 comprises a convolutional encoder 14004, a bit interleaving and mapping module 14006, an inverse FFT module 14008, a symbol shaping module 14002, a PSK/QAM modulation transmitter 14012, and an antenna 14024. The structure and operation of transmit OFDM PMD 14000 will be further described as follows, and is further described elsewhere herein.

Convolutional encoder 14004 receives a PPDU signal 14014. In embodiments, PPDU signal 14014 may comprise one or more PPDU frames, and/or PPDU frame portions, to be modulated according to PSK or QAM modulation schemes. For instance, PPDU signal 14014 may comprise the PLCP preamble and/or signal field, which may be modulated according to BPSK modulation. Furthermore, PPDU signal 14014 may comprise one or more data fields, which may be modulated according to BPSK, QPSK, 16-QAM, and 64-QAM. Alternatively, the OFDM PMD PLCP

preamble, signal field, and data fields may be modulated according to any of the modulation schemes described herein.

Convolutional encoder 14004 encodes the PPDU signal 14014, and outputs an encoded PPDU signal 14016. The design and use of a convolutional encoder 14004 is well known to those skilled in the relevant art(s). A suitable convolutional encoder 14004 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Bit interleaving and mapping module 14006 receives encoded PPDU signal 14016. Bit interleaving and mapping module 14006 maps encoded PPDU signal 14016, and outputs mapped signal 14018. The design and use of a bit interleaving and mapping module 14006 is well known to those skilled in the relevant art(s). A bit interleaving and mapping module 14006 may be designed and implemented in software, firmware, hardware, and any combination thereof.

Inverse FFT module 14008 receives mapped signal 14018. Inverse FFT module 14008 performs an inverse FFT upon mapped signal 14018, and outputs IFFT signal 14020. The design and use of an inverse FFT module 14008 is well known to those skilled in the relevant art(s). A suitable inverse FFT module 14008 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Symbol shaping module 14010 receives IFFT signal 14020. Symbol shaping module shapes IFFT signal 14020, and outputs shaped signal 14022. The design and use of a symbol shaping module 14010 is well known to those skilled in the relevant art(s). A suitable symbol shaping module 14010 may be designed and implemented in software, firmware, hardware, and any combination thereof.

PSK/QAM modulation transmitter 14012 receives shaped signal 14022. PSK/QAM modulation transmitter 14012 modulates one or more oscillating signals with shaped signal 14022 according to BPSK, QPSK, or QAM modulation techniques, and frequency up-converts shaped signal 14022. PSK/QAM modulation transmitter 14012 outputs transmitted modulated signal 14026, which is transmitted by antenna 14024.

The transmit OFDM PMD of FIG. 140A may incorporate universal frequency translation technology to provide for modulation and frequency up-conversion of WLAN station signals. For example, OFDM PMD 14000 may use universal frequency translation technology to modulate signals according to BPSK, QPSK, and QAM modulation techniques. FIG. 140C illustrates an exemplary embodiment of the PSK/QAM modulation transmitter 14012 of FIG. 140A. Transmitter 14012 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Transmitter 14012 of FIG. 140C comprises at least one UFT module 12810. UFT module 12810 provides for modulation and frequency up-conversion of WLAN station signals to be transmitted. As described above, transmit OFDM PMD 14000 transmits the PLCP preamble and signal field at 6 Mbps using BPSK, and the data fields are sent at the rates and modulation schemes shown in Table 6 above, depending on the content in the signal field. Numerous embodiments for transmitter 14012 will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for transmitter 14012 incorporating UFT module 12810 are further described below and elsewhere herein.

6.7.1.5.1.1 UFU Module Transmitter Embodiments for BPSK Modulation

FIG. 140D illustrates in greater detail an exemplary embodiment of transmitter 14012 of FIG. 140A. Transmitter 14012 comprises a PSK modulator 14001, a UFU module 12812, and an optional amplifier 14003.

PSK modulator 14001 of transmitter 14012 receives a shaped signal 14022. PSK modulator 14001 modulates shaped signal 14022, according to binary phase shift keying (BPSK) modulation. For example, PSK modulator 14001 may frequency modulate an oscillating signal using filtered

signal 14022. PSK modulators are well known to persons skilled in the relevant art(s). PSK modulator 14001 outputs modulated signal 14005. The design and use of a PSK modulator 14001 is well known to those skilled in the relevant art(s). A suitable PSK modulator 14001 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Modulated signal 14005 is received by UFU module 12812. UFU module 12812 includes at least one UFT module 12810. UFU module 12812 frequency up-converts modulated signal 14005, and outputs UFU module output signal 14007. Various structures and methods for operation of UFU module 12812 are described more fully elsewhere herein. For example, Section 6.6.2.6.1.1.1 provides an exemplary structural and operational description of an embodiment of UFU module 12812 in FIG. 129E, where in the present PSK embodiment, modulated signal 14005 is input to pulse shaping circuit 12954. Hence, each of the harmonics of harmonically rich signal 12966 have frequency proportional to control signal 12964, and in a PSK embodiment are thus considered to be PSK modulated.

When present, optional amplifier 14003 amplifies UFU module output signal 14007, outputting transmitted modulated signal 14026. Transmitted modulated signal 14026 comprises a BPSK modulated signal.

Further embodiments for up-converting PSK modulated signals are described in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998, the full disclosure of which is incorporated herein by reference in its entirety.

6.7.1.5.1.2 BPSK Balanced Modulator Transmitter Embodiments

Balanced modulator transmitter configurations are presented in Section 3.1. These transmitter configurations may be applied in transmitter 14012 of FIG. 140A to modulate and frequency up-convert WLAN station signals according to PSK modulation techniques. The balanced modulator transmitter configurations presented above and applicable to transmitter 14012 include

transmitter 7102 of FIG. 71A, transmitter 7162 of FIG. 71D, transmitter 7302 of FIG. 73A, and transmitter 7900 of FIG. 79A. Refer to Section 3.1 above for detailed description of these transmitters. Further details pertaining to balanced modulator transmitters are provided in co-pending U.S. Patent Application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Serial No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. 140E illustrates balanced modulator embodiments for transmitter 14012, according to the present invention. Transmitter 14012 comprises a PSK modulator 14009 and a transmitter 7102, 7162, 7302, 7900. Further balanced modulator embodiments for transmitter 14012 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

PSK modulator 14009 receives shaped signal 14022. PSK modulator 14009 produces an oscillating signal modulated with shaped signal 14022 according to PSK modulation. PSK modulator 14009 outputs PSK modulated signal 14011. The design and use of a PSK modulator 14009 is well known to those skilled in the relevant art(s). A suitable PSK modulator 14009 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Transmitter 7102, 7162, 7302, 7900 receives PSK modulated signal 14011. PSK modulated signal 14011 of FIG. 140E corresponds to baseband signal 7110 of FIGS. 71A and 71D, baseband signal 7306 of FIG. 73A, and baseband signal 7902 of FIG. 79A. Transmitter 7102, 7162, 7302, 7900 may be one of transmitter 7102 of FIG. 71A, transmitter 7162 of FIG. 71D, transmitter 7302 of FIG. 73A, and transmitter 7900 of FIG. 79A, and other balanced modulator transmitter of the present invention described herein. The one of transmitters 7102, 7162, 7302, 7900 selected for a particular implementation of transmitter 14012 will depend on the particular application. Transmitter 7102, 7162, 7302, 7900 frequency up-converts PSK modulated signal 14011, and outputs transmitted modulated signal 14026. Transmitted modulated signal 14026 of FIG. 140E corresponds to output signal 7140 of FIGS. 71A and 71D, output signal 7322 of FIG. 73A, and

output signal 7936 of FIG. 79A. Transmitted modulated signal 14026 comprises a BPSK modulated information signal.

6.7.1.5.1.3 QPSK/QAM Modulation Mode Transmitter Embodiments

Embodiments are provided below for implementing QPSK and QAM modulation transmitters and receivers that may be implemented in WLAN stations, according to embodiment of the present invention. For example, the QPSK and QAM modulation transmitters described below may be implemented in transmit OFDM PMD sublayer 14000 to transmit QPSK and QAM modulated WLAN signals. These transmitter embodiments are described herein for purposes of illustration, and not limitation. Alternate transmitter embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.7.1.5.1.3.1 QPSK Modulation Mode Transmitter Embodiments

FIGS. 129G-129I illustrate exemplary DQPSK modulation transmitter configurations related to transmitter 12910 of FIG. 129A, according to embodiments of the invention. The DQPSK modulation transmitter configurations of FIGS. 129G-129I are adaptable to providing for QPSK modulation in transmitter 14012 of FIG. 140A, according to further embodiments of the present invention. For instance, referring to FIG. 129G, in a QPSK modulation embodiment, DQPSK modulation transmitter 12978 may be adapted to a QPSK modulation transmitter. As a result, transmitted modulated signal 12924 is a QPSK modulated signal. Referring to FIG. 129H, in a QPSK modulation embodiment, first and second DBPSK modulators 12909 and 12980 may be

adapted to first and second BPSK modulators, respectively. As a result, first and second DBPSK modulated signals 12901 and 12975 are BPSK modulated signals. Referring to FIG. 129I, in a QPSK modulation embodiment, first and second DBPSK modulators 12911 and 12913 are adapted to first and second BPSK modulators, respectively. As a result, first and second DBPSK modulated signals 12977 and 12979 are BPSK modulated signals.

Hence, the DQPSK modulation transmitter configurations of FIGS. 129G-129I may be referred to for exemplary QPSK modulation embodiments of transmitter 14012. Refer to Section 6.6.2.6.1.3 for further description of the structure and operation of the DQPSK modulation transmitter configurations of FIGS. 129G-129I. Alternate QPSK modulation transmitter embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.7.1.5.1.3.2 QAM Modulation Mode Transmitter Embodiments

Quadrature Amplitude Modulation (QAM) is a well known technique for modulating digital signals using both amplitude and phase coding. Multiple signals may be transmitted using quadrature carriers. An in-phase signal ("I") is modulated such that its amplitude varies discretely as a function of one of the information signals, and a quadrature-phase signal ("Q") is modulated such that its amplitude varies discretely as a function of the other information signal. The two modulated signals are combined to form an "QAM" modulated signal and transmitted. In this manner, for instance, two separate information signals could be transmitted in a single signal simultaneously. For determining the number of possible discrete levels, M-QAM utilizes a signal structure where each data signal may take on the square-root of M different possible levels. In 64-QAM, each information signal is modulated with the carrier signal in 3 bit segments. Hence, 6 bits

are transmitted per symbol. In 16-QAM, each information signal is modulated with the carrier signal in 2 bit segments. Hence, 4 bits are transmitted per symbol.

Embodiments are provided below for implementing QAM transmitters and receivers that may be implemented in IEEE Std. 802.11 WLAN implementations, according to embodiments of the present invention.

FIG. 140F illustrates an exemplary block diagram of a transmitter 14012 operating in a QAM modulation mode, according to an embodiment of the present invention. Transmitter 14012 of FIG. 140F comprises a signal separator 14048 and a QAM transmitter 14050.

Signal separator 14048 receives shaped signal 14022 and outputs I information signal 14052 and Q information signal 14054. When shaped signal 14022 is a bused signal, signal separator 14048 may merely be a location on the bus where shaped signal 14022 is diverges into separate buses or data signals, for instance. Signal separator 14048 may alternatively comprise logic and memory for receiving and storing shaped signal 14022, and logically dividing it into the two signals. A suitable signal separator 14048 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

QAM transmitter 14050 receives I information signal 14052 and Q information signal 14054. QAM transmitter 14050 provides QAM modulation to I information signal 14052 and Q information signal 14054, outputting transmitted modulated signal 14026. Methods and structures related to QAM transmitter 14012, including methods and structures related to QAM transmitter 14050, are described in more detail in the following sections.

QAM transmitter 14050 comprises at least one UFT module 12810. Numerous embodiments for QAM transmitter 14050 will be recognized by persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. In embodiments, UFT module 12810 frequency up-converts an input signal to an RF signal. Methods and structures related to UFT module 12810 are described more fully in the following sections.

6.7.1.5.1.3.2.1 ***QAM Modulation Transmitter Using Two UFU Modules***

FIG. 140G illustrates a more detailed circuit block diagram for QAM transmitter 14050. QAM transmitter 14050 up-converts and modulates an input signal according to QAM modulation techniques. QAM transmitter 14050 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

QAM transmitter 14050 comprises a first digital-to-analog (D/A) converter 14019, a second D/A converter 14021, a first UFU module 14056, a second UFU module 14058, an oscillator 14060, a phase shifter 14062, a summer 14064, and a filter 14066.

First D/A converter 14019 receives I phase information signal 14052. First D/A converter 14019 outputs an I phase n-level signal 14023 with an amplitude that varies according to the value of I phase information signal 14052. For example, in a 64-QAM embodiment, n is equal to 8. I phase information signal 14052 is a digital signal that first D/A converter 14019 converts to an analog signal, in 3 bit segments. Each 3 bit segment of I phase information signal 14052 is converted to an analog signal with 8 possible discrete levels, such as ±a, ±3a, ±5a, and ±7a, wherein "a" is equal to any applicable voltage value, such as .5 V. Other voltage values are within the scope of the present invention. In a 16-QAM embodiment, n is equal to 4. I phase information signal 14052 is converted to I phase n-level signal 14023 in 2 bit segments. Each 2 bit segment of I phase information signal 14052 is converted to an analog signal with 4 possible discrete levels. Other m-QAM types are within the scope of the present invention.

Second D/A converter 14021 receives Q phase information signal 14054. Second D/A converter 14021 outputs an Q phase n-level signal 14025 with an amplitude that varies according to the value of Q phase information signal 14054. For example, in a 64-QAM embodiment, n is

equal to 8. Q phase information signal 14054 is a digital signal that second D/A converter 14021 converts to an analog signal, in 3 bit segments. Each 3 bit segment of Q phase information signal 14054 is converted to an analog signal with 8 possible discrete levels, such as ±a, ±3a, ±5a, and ±7a, wherein "a" is equal to any applicable voltage value, such as .5 V. Other voltage values are within the scope of the present invention. In a 16-QAM embodiment, n is equal to 4. Q phase information signal 14054 is converted to Q phase n-level signal 14025 in 2 bit segments. Each 2 bit segment of Q information signal 14054 is converted to an analog signal with 4 possible discrete levels. Other m-QAM types are within the scope of the present invention.

The design and use of first and second D/A converters 14019 and 14021 are well known to those skilled in the relevant art(s). Suitable first and second D/A converters 14019 and 14021 may be designed and implemented in software, firmware, hardware, and any combination thereof, or may be purchased "off the shelf." First and second D/A converters 14019 and 14021 may not be required if I phase information signal 14052 and Q phase information signal 14054 are already n-level signals due to operation of a prior stage of PSK/QAM modulation transmitter 14012.

Oscillator 14060 generates an "I"-oscillating signal 14084.

I phase n-level signal 14023 is input to first UFU module 14056. First UFU module 14056 comprises a first UFT module 14068, a first resistor 14067, and a first voltage reference 14080. I phase n-level signal 14023 is preferably a first data signal with multiple discrete voltage values. The "I"-oscillating signal 14084 is modulated by I phase n-level signal 14023 in first UFU module 14056, thereby producing an "I"-modulated signal 14088. First UFT module 14068 comprises a first switch 14072. As first switch 14072 opens and closes, it gates I phase n-level signal 14023. The result of the gating is a harmonically rich "I" signal 14088 having a fundamental frequency substantially proportional to "I"-oscillating signal 14084 and an amplitude substantially proportional to the amplitude of I phase n-level signal 14023. Each of the harmonics of the harmonically rich "I" signal also have amplitudes proportional to the I phase n-level signal 14023, and are thus considered to be amplitude modulated.

The phase of "I"-oscillating signal 14084 is shifted by phase shifter 14062 to create "Q"-oscillating signal 14086. Phase shifter 14062 preferably shifts the phase of "I"-oscillating signal 14084 by 90 degrees.

Q phase n-level signal 14025 is input to second UFU module 14058. Second UFU module 14058 comprises a second UFT module 14070, a second resistor 14078, and a second voltage reference 14082. Q phase n-level signal 14025 is preferably a second data signal with multiple discrete voltage values similar to those of I phase n-level signal 14023. "Q"-oscillating signal 14086 is modulated by Q phase n-level signal 14025 in second UFU module 14056, thereby producing an "Q"-modulated signal 14090. Second UFT module 14070 comprises a second switch 14074. As second switch 14074 opens and closes, it gates Q phase n-level signal 14025. The result of the gating is a harmonically rich "Q" signal 14090 having a fundamental frequency substantially proportional to "Q"-oscillating signal 14086 and an amplitude substantially proportional to the amplitude of Q phase n-level signal 14025. Each of the harmonics of the harmonically rich "Q" signal also have amplitudes proportional to the Q phase n-level signal 14025, and are thus considered to be amplitude modulated.

Harmonically rich "I" signal 14088 and harmonically rich "Q" signal 14090 are preferably rectangular waves, such as square waves or pulses (although the invention is not limited to this embodiment), and are comprised of pluralities of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveforms. These sinusoidal waves are referred to as the harmonics of the underlying waveforms, and a Fourier analysis will determine the amplitude of each harmonic.

Harmonically rich "I" signal 14088 and harmonically rich "Q" signal 14090 are combined by summer 14064 to create harmonically rich "QAM" signal 14092. Summers are well known to persons skilled in the relevant art(s).

Filter 14066 filters out the undesired harmonic frequencies, and outputs a transmitted modulated signal 14026 at the desired harmonic frequency or frequencies.

It will be apparent to persons skilled in the relevant art(s) that an alternative embodiment exists wherein the harmonically rich "I" signal 14088 and the harmonically rich "Q" signal 14090 may be filtered before they are summed. Other "QAM"-modulation embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

6.7.1.5.1.3.2.2 QAM Modulation Transmitter Using Balanced Modulator

I/Q balanced modulator transmitter configurations are presented in Section 3.2. These transmitter configurations may be applied in transmitter 14012 to modulate and frequency up-convert WLAN station signals according to QAM modulation techniques. The I/Q balanced modulator transmitter configurations presented above and applicable to transmitter 14012 include I/Q transmitter 7420 of FIG. 74, I/Q transmitter 7608 of FIG. 76A, I/Q transmitter 7618 of FIG. 76B, I/Q transmitter 7702 of FIG. 77, I/Q transmitter 7802 of FIG. 78, I/Q transmitter 8000 of FIG. 80, I/Q transmitter 8200 of FIG. 82, and I/Q transmitter 8300 of FIG. 83. Refer to Section 3.2 above for detailed description of these transmitters. Further details pertaining to I/Q balanced modulator transmitters are provided in co-pending U.S. Patent Application entitled "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Serial No. 09/525,615, which is incorporated herein by reference in its entirety.

FIG. 140H illustrates I/Q balanced modulator embodiments for QAM modulation transmitter 14050, according to the present invention. QAM modulation transmitter 14050 comprises a first amplitude modulator 14094, a second amplitude modulator 14096, a pulse generator 7144, and an I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300. Further I/Q balanced modulator embodiments for QAM modulation transmitter 14050 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

For instance, QAM transmitter 14050 may comprise D/A converters such as first and second D/A converters 14019 and 14021 shown in FIG. 140G to convert I phase information signal 14052 and Q phase information signal 14054 to n-level signals, if required.

First amplitude modulator 14094 receives I phase information signal 14052. First amplitude modulator 14094 produces a signal amplitude modulated with I phase information signal 14052. First amplitude modulator 14094 outputs first amplitude modulated signal 14013.

Second amplitude modulator 14096 receives Q phase information signal 14054. Second amplitude modulator 14015 produces a signal amplitude modulated with Q phase information signal 14054. Second amplitude modulator 14096 outputs second amplitude modulated signal 14015. The design and use of a first and second amplitude modulator 14094 and 14096 is well known to those skilled in the relevant art(s). Suitable first and second amplitude modulators 14094 and 14096 may be designed and implemented in software, firmware, hardware, and any combination thereof, or may be purchased "off the shelf."

Pulse generator 7144 generates control signals 7123 and 7127 as described elsewhere herein.

I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300 receives first amplitude modulated signal 14013, second amplitude modulated signal 14015, and control signals 7123 and 7127. First amplitude modulated signal 14013 of FIG. 140H corresponds to I baseband signal 7402 of FIGS. 74, 76A, 76B, 77, and 78, and I baseband signal 8002 of FIGS. 80, 82, and 83. I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300 may be one of I/Q transmitter 7420 of FIG. 74, I/Q transmitter 7608 of FIG. 76A, I/Q transmitter 7618 of FIG. 76B, I/Q transmitter 7702 of FIG. 77, I/Q transmitter 7802 of FIG. 78, I/Q transmitter 8000 of FIG. 80, I/Q transmitter 8200 of FIG. 82, and I/Q transmitter 8300 of FIG. 83, and other I/Q balanced modulator transmitter of the present invention described herein. The one of I/Q transmitters 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300 selected for a particular implementation of transmitter 14012 will depend on the particular application. I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300 combines and frequency up-converts first and second amplitude modulated signals 14013 and 14015, and outputs transmitted modulated signal 14026. Transmitted modulated signal 14026 of FIG. 140H

corresponds to output signal 7148 of FIGS. 74, 76A, 76B, 77, and 78, and output signal 8016 of FIGS. 80, 82, and 83. Transmitted modulated signal 14026 comprises a QAM modulated information signal.

6.7.1.5.2 Receiver OFDM PMD Incorporating Universal Frequency Translation

As shown in FIG. 140B, receiver OFDM PMD 14002 comprises an antenna 14038, a PSK/QAM modulation receiver 14028, a FFT module 14030, a bit de-interleaving and de-mapping module 14032, a convolutional code decoder 14034, and an AFC and clock recovery module 14036. The structure and operation of receiver OFDM PMD 14002 will be further described as follows, and is further described elsewhere herein.

Antenna 14038 receives a transmitted modulated signal 14026. Transmitted modulated signal 14026 comprises an RF carrier signal modulated with an information signal according to QAM modulation techniques.

PSK/QAM modulation receiver 14028 receives transmitted modulated signal 14026. PSK/QAM modulation receiver 14028 demodulates and down-converts transmitted modulated signal 14026, and outputs demodulated signal 14040.

FFT module 14030 receives demodulated signal 14040. FFT module 14030 performs an FFT on demodulated signal 14040, and outputs FFT output signal 14042. The design and use of a FFT module 14030 is well known to those skilled in the relevant art(s). A FFT module 14030 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Bit de-interleaving and de-mapping module 14032 receives FFT output signal 14042. Bit de-interleaving and de-mapping module 14032 de-interleaves and de-maps FFT output signal 14042, and outputs de-mapped signal 14044. The design and use of a bit de-interleaving and de-mapping module 14032 is well known to those skilled in the relevant art(s). A suitable bit de-interleaving and

de-mapping module 14032 may be designed and implemented in software, firmware, hardware, and any combination thereof.

Convolutional code decoder 14034 receives de-mapped signal 14044. Convolutional code decoder 14034 decodes de-mapped signal 14044, and outputs PPDU signal 14046. PPDU signal 14034 comprises one or more PPDU frames and/or PPDU frame portions, such as a PLCP preamble, signal field, and data field. The design and use of a convolutional code decoder 14034 is well known to those skilled in the relevant art(s). A suitable convolutional code decoder 14034 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

AFC and clock recovery module 14036 is coupled to PSK/QAM de-modulator 14028. AFC and clock recovery module 14036 may be used to recover clocking/timing information from the received signal. AFC and clock recovery module 14036 may output a data clock signal, and may pass clocking/timing information back to PSK/QAM de-modulator 14028. The design and use of an AFC and clock recovery module 14036 is well known to those skilled in the relevant art(s). A suitable AFC and clock recovery module 14036 may be designed and implemented in software, firmware, hardware, and any combination thereof.

Alternate embodiments for receiver OFDM PMD 14002 will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

The receiver OFDM PMD 14002 of FIG. 140B may incorporate universal frequency translation technology to provide for demodulation and frequency down-conversion of received WLAN station signals. FIG. 140I illustrates an exemplary embodiment of the PSK/QAM modulation receiver 14028 of FIG. 140B. Receiver 14028 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver 14028 of FIG. 140I comprises at least one UFT module 12810. UFT module 12810 provides for demodulation and frequency down-conversion of received WLAN station signals. As described above, receiver OFDM PMD 14002 demodulates the BPSK-modulated PLCP preamble and signal field, and demodulates the BPSK-, QPSK-, 16-QAM-, or 64-QAM- modulated data field. Numerous embodiments for receiver 14028 will be known to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Embodiments for receiver 14028 incorporating UFT module 12810 are further described below and elsewhere herein.

6.7.1.5.2.1 UFD Module Receiver Embodiments for BPSK Demodulation

Various embodiments for receiver 14028 exist, where receiver 14028 comprises one or more UFD modules, and are described elsewhere herein. For instance, receiver 14028 may comprise a UFD module 12814, as shown in FIGS. 128C and 128D. These embodiments are adaptable to demodulation of BPSK modulated signals such as transmitted modulated signal 14026.

For example, Section 6.6.2.6.2.1 provides exemplary structural and operational description of embodiments comprising a UFD module 12814 for signal down-conversion and demodulation. The configurations shown in FIGS. 129M and 129N for receiver 12930 are adaptable to receiver 14028 for down-conversion of BPSK modulated WLAN signals. Receiver 14028 may be configured as shown for receiver 12930 in FIGS. 129M and 129N to down-convert and demodulate transmitted modulated signal 14040. As described above, transmitted modulated signal 14040 is modulated according to BPSK.

In the demodulator configurations of FIG. 129M and 129N, transmitted modulated signal 14040 is input to UFD module 12814. UFD module 12814 frequency down-converts and demodulates transmitted modulated signal 14040 to UFD module output signal 12921. In the embodiment shown in FIG. 129M, UFD module 12814 frequency down-converts transmitted modulated signal 14040 to a baseband signal. In the embodiment shown in FIG. 129N, UFD module

12814 down-converts transmitted modulated signal 14040 to an intermediate frequency. Demodulated signal 12940 of FIGS. 129M and 129N corresponds to demodulated signal 14040 of FIG. 140B. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Various structures and methods for operation of UFD module 12814 are described more fully elsewhere herein. For example, Section 6.6.2.6.2.1.1 provides an exemplary structural and operational description of an embodiment of UFD module 12814, shown in FIG. 129O, where in a BPSK embodiment, transmitted modulated signal 14040 is input to UFT module 12810.

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6.7.1.5.2.2 BPSK Single Channel Receiver Embodiments

Single channel balanced receiver configurations are presented in Section 2.2.3. These receiver configurations may be applied in receiver 14028 to demodulate and frequency down-convert WLAN station signals according to BPSK demodulation techniques. The single channel balanced receiver configurations presented above and applicable to receiver 14028 include receiver 11900 of FIG. 119. Refer to Section 2.2 above for detailed description of these receivers. Further details pertaining to balanced modulator receivers are provided in co-pending U.S. Patent Application entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Serial No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. 140J illustrates a single channel balanced demodulator embodiment for receiver 14028, according to the present invention. Receiver 14028 comprises a single channel receiver 11900. Further single channel balanced demodulator embodiments for receiver 14028 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Receiver 11900 receives transmitted modulated signal 14026. Transmitted modulated signal 14026 of FIG. 140J corresponds to input RF signal 11906 of FIG. 119. Receiver 11900 frequency down-converts and demodulates transmitted modulated signal 14026, and outputs demodulated signal 14040. Demodulated signal 14040 of FIG. 140J corresponds to baseband output signal 11908 of FIG. 119. Demodulated signal 14040 comprises an information signal.

6.7.1.5.2.3 QPSK/QAM Modulation Mode Receiver Embodiments

FIG. 140K illustrates an exemplary QPSK and QAM modulation mode embodiment of receiver 14028, according to the present invention. This QPSK/QAM modulation mode receiver embodiment is described herein for purposes of illustration, and not limitation. Alternate QPSK and QAM modulation mode receiver embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

Receiver 14028 comprises a QPSK/QAM modulation receiver 14098. QPSK/QAM modulation receiver 14098 down-converts and demodulates an input signal that is modulated according to QPSK or QAM modulation techniques. QPSK/QAM modulation receiver 14098 down-converts and demodulates a received input signal to two baseband information signals. QPSK/QAM modulation receiver 14098 comprises at least one UFT module 12810. QPSK/QAM modulation receiver 14098 provides for QPSK and QAM demodulation to transmitted modulated signal 14026, outputting demodulated signal 14040. Numerous embodiments for QPSK/QAM modulation receiver 14098 will be recognized by persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the invention. Various embodiments for QPSK/QAM modulation receiver 14098 are provided in the following subsections.

6.7.1.5.2.3.1 QPSK/QAM Modulation Receiver Using Two UFD Modules

QPSK modulation receiver 12939 shown in FIG. 129R is adaptable to down-converting and demodulating QPSK and QAM modulated signals. Accordingly, the configuration of QPSK modulation receiver 12939 may be applied to QPSK/QAM modulation receiver 14098. The structure and operation of QPSK modulation receiver 12939 is further described as follows, as applied to a QPSK and QAM modulation environment of QPSK/QAM modulation receiver 14098.

Receiver 12930 comprises an oscillator 12949, a first UFD module 12941, a second UFD module 12943, a first UFT module 12945, a second UFT module 12947, a phase shifter 12951, a first optional amplifier 12953, a first filter 12955, a second optional amplifier 12957, and a second filter 12959.

De-spread signal 12938 of FIG. 129R corresponds to transmitted modulated signal 14026 of FIG. 140K. As described above, transmitted modulated signal 14026 may comprise a QPSK or QAM modulated signal. Transmitted modulated signal 14026 is received by first UFD module 12941 and second UFD module 12943.

Oscillator 12949 provides an oscillating signal used by both first UFD module 12941 and second UFD module 12943 via the phase shifter 12951. Oscillator 12949 generates an "I" oscillating signal 12961.

"I" oscillating signal 12961 is input to first UFD module 12941. First UFD module 12941 comprises at least one UFT module 12945. In an embodiment, first UFD module 12941 is structured similarly to UFD module 12814 of FIG. 129O, with oscillator 12949 substituting for oscillator 12927, and "I" oscillating signal 12961 substituting for oscillating signal 12935. First UFD module 12941 frequency down-converts and demodulates de-spread signal 12938 to down-converted "I" signal 12965 according to "I" oscillating signal 12961. In a QPSK modulation embodiment, down-converted "I" signal 12965 may be an information signal with two possible states or voltage levels. In a QAM modulation embodiment, down-converted "I" signal 12965 may be an information signal

with more than two possible states or voltage levels. For instance, in 16-QAM, down-converted "I" signal 12965 may have 4 states or levels, and in 64-QAM, may have 8 states or levels.

Phase shifter 12951 receives "I" oscillating signal 12961, and outputs "Q" oscillating signal 12963, which is a replica of "I" oscillating signal 12961 shifted preferably by 90°.

Second UFD module 12943 inputs "Q" oscillating signal 12963. Second UFD module 12943 comprises at least one UFT module 12947. In an embodiment, second UFD module 12943 is structured similarly to UFD module 12814 of FIG. 129O with "Q" oscillating signal 12963 substituting for oscillating signal 12935. Second UFD module 12943 frequency down-converts and demodulates de-spread signal 12938 to down-converted "Q" signal 12967 according to "Q" oscillating signal 12963. In a QPSK modulation embodiment, down-converted "Q" signal 12967 may be an information signal with two possible states or voltage levels. In a QAM modulation embodiment, down-converted "Q" signal 12967 may be an information signal with more than two possible states or voltage levels. For instance, in 16-QAM, down-converted "Q" signal 12967 may have 4 states or levels, and in 64-QAM, may have 8 states or levels.

Down-converted "I" signal 12965 is optionally amplified by first optional amplifier 12953 and optionally filtered by first optional filter 12955, and a first information output signal 12969 is output.

Down-converted "Q" signal 12967 is optionally amplified by second optional amplifier 12957 and optionally filtered by second optional filter 12959, and a second information output signal 12971 is output.

In an embodiment of QPSK/QAM modulation receiver 14098, first information output signal 12969 and second information output signal 12971 depicted in FIG. 129R comprise demodulated signal 14040 of FIG. 140K.

Alternate configurations for QPSK/QAM modulation receiver 14028 will be apparent to persons skilled in the relevant art(s) from the teachings herein. For instance, an alternate embodiment exists wherein phase shifter 12951 is coupled between transmitted modulated signal 14026 (de-spread signal 12938 of FIG. 129R) and UFD module 12943, instead of the configuration

described above. This and other such QPSK/QAM modulation mode receiver embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

6.7.1.5.2.3.2 QPSK/QAM Modulation Receiver Using Balanced Demodulator

I/Q balanced demodulator receiver configurations are presented in Section 2.2. These receiver configurations may be applied in demodulator 14098 to demodulate and frequency down-convert WLAN station signals according to QPSK and QAM demodulation techniques. The I/Q balanced demodulator receiver configurations presented above and applicable to receiver 14028 include I/Q modulation receiver 10300 of FIG. 103. Refer to Section 2.2 above for detailed description of this receiver. Further details pertaining to I/Q balanced demodulator receivers are provided in co-pending U.S. Patent Application entitled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Serial No. 09/526,041, which is incorporated herein by reference in its entirety.

FIG. 140L illustrates I/Q balanced demodulator embodiments for QPSK/QAM modulation receiver 14098 of FIG. 104K, according to the present invention. QPSK/QAM modulation receiver 14098 comprises a control signal generator 14017 and an I/Q modulation receiver 10300 of FIG. 103. Further I/Q balanced demodulator embodiments for QPSK/QAM modulation receiver 14098 will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

Control signal generator 14017 generates control signals 10390, 10392, 10394 and 10396 as described elsewhere herein. Control signal generator 14017 may comprise a variety of control signal/pulse generator configurations as described elsewhere herein, including control signal generator 10400 of FIG. 104.

I/Q modulation receiver 10300 receives transmitted modulated signal 14026 and control signals 10390, 10392, 10394 and 10396. Transmitted modulated signal 14026 corresponds to I/Q

modulated RF input signal 10382 of FIG. 103. I/Q modulation receiver 10300 demodulates and frequency down-converts transmitted modulated signal 14026, and outputs I baseband output signal 10384 and Q baseband output signal 10386, which form demodulated signal 14040. Demodulated signal 14040 comprises I baseband output signal 10384 and Q baseband output signal 10386.

6.7.1.6 OFDM Operating Channels and Transmit Power Requirements

The 5 GHz U-NII frequency band is segmented into three 100 MHZ bands for operation in the United States. The lower band ranges from 5.15-5.25 GHz, the middle band ranges from 5.25-5.35 GHz and the upper band ranges from 5.725-5.825 GHz. The lower and middle bands accommodate 8 channels in a total bandwidth of 200 MHZ and the upper band accommodates 4 channels in a 100 MHZ bandwidth. The frequency channels center frequencies are spaced 20 MHZ apart. The outermost channels of the lower and middle bands are centered 30 MHZ from the outer edges. In the upper band, the outermost channel centers are 20 MHZ from the outer edges. The channel frequencies and numbering defined in IEEE 802.11a start at 5 GHz, and each channel is spaced 5 GHz apart. A set of channel frequencies for each of the U-NII bands is defined in Table 7.

Regulatory Domain	Frequency Band	Channel Number	Center Frequencies
USA	U-NII lower band 5.15-5.25 GHz	36 40 44 48	5.180 GHz 5.220 GHz 5.220 GHz 5.240 GHz
USA	U-NII middle band 5.25-5.35 GHz	52 56 60 64	5.260 GHz 5.280 GHz 5.300 GHz 5.320 GHz
USA	U-NII upper band 5.725-5.825 GHz	149 153 157 161	5.745 GHz 5.765 GHz 5.785 GHz 5.805 GHz

Table 7

In addition to frequency and channel allocations, transmit power is a key parameter regulated in the 5 GHz U-NII frequency band. Three transmit RF power levels are specified: 40 mW, 200 mW and 800 mW, as illustrated in Table 8. The upper band defines RF transmit power levels suitable for bridging applications. The lower band specifies a transmit power level suitable for short-range indoor home and small office environments.

Frequency Band	Maximum Transmit Power with 6 dBi Antenna Gain
5.150-5.250 GHz	40 mW (2.5 mW/MHZ)
5.250-5.350 GHz	200 mW (12.5 mW/MHZ)
5.725-5.825 GHz	800 mW (50 mW/MHZ)

Table 8

6.7.1.7 Geographic Regulatory Bodies

WLAN IEEE 802.11a-compliant OFDM radios operating in the 5 GHz UNII frequency band must comply with the local geographical regulatory domains regarding this spectrum. Such products may be subject to certification. For example, regulatory agencies may set emission standards for WLANs in order to minimize the amount of interference a radio may generate or may receive from a nearby radio. The regulatory requirements do not affect the interoperability of IEEE 802.11a compliant products. In the United States, the FCC has responsibility for the allocation of 5 GHz U-UNII bands.

6.7.1.7.1 North America

Geographic Area: USA

Approval Standards: Federal Communications Commission (FCC) Documents: CFR47, Part 15; Sections 15.205,15.209, and subpart E;

Sections 15.401-15.407

Approval Authorities: Federal Communications Commission (FCC)

6.7.1.8 Globalization of Spectrum at 5 GHz

IEEE 802.11, ETSI's HIPERLAN II, and Japan's Mobile Multimedia Access Communication Promotion Council (MMAC-PC) have pursued available spectrum allocations in the 5 GHz band. In Europe, the 5.15-5.35 GHz frequency band is reserved for HIPERLAN II devices. ETSI-HIPERLAN II and IEEE 802.11 may potentially share the lower 5 GHz band, drawing on the extreme similarity of the PHY layers of both projects. In Japan, the Wireless Ethernet Working Group of the MMAC-PC recommends using the 802.11a standard at the time the 5.15-5.25 GHz band becomes available in Japan.

6.7.2 IEEE 802.11b-2.4 High Rate DSSS PHY

The IEEE 802.11b PHY extension of IEEE 802.11 is referred to as high rate direct sequence spread spectrum (HR/DSSS). The HR/DSSS PHY provides two functions: First, the HR/DSSS extends the PSDU data rates to 5.5 Mbps and 11 Mbps using an enhanced modulation technique. Second, the HR/DSSS PHY provides a rate shift mechanism, which allows 11 Mbps networks to fall back to 1 and 2 Mbps and interoperate with the legacy IEEE 802.11 2.4 GHz RF PHY layers. The OSI structure and operation of the PHY's PLCP sublayer and PMD sublayer for HR/DSSS is similar to the existing IEEE 802.11 DSSS PHY described herein. The following sections give an overview of the PLCP header, data rates, and modulations defined in IEEE 802.11b. The HR/DSSS PHY of the present invention may incorporate universal frequency translation technology for WLAN signal up-conversion, down-conversion, modulation, and de-modulation, as described in subsequent sub-sections.

6.7.2.1 HR/DSSS PHY PLCP Sublayer

A PPDU frame consists of the PLCP preamble, PLCP header, and the PSDU. As with IEEE 802.11 DSSS, the PMD uses the PLCP preamble to acquire the incoming signal and synchronize the receiver's demodulator. The HR/DSSS PHY defines two PLCP preambles, long and short. FIG. 141A illustrates a PPDU with a long PLCP preamble 14102. FIG. 141B illustrates a PPDU with a short preamble 14104. The long preamble 14102 uses the same PLCP preamble and header as used by the IEEE 802.11 DSSS PHY, and sends the information at 1 Mbps using DBPSK and Barker word direct sequence spreading. The PSDU is transmitted at 1, 2, 5.5, and 11 Mbps as determined by the content in the signal field. The long preamble 14102 is backwards compatible with existing IEEE 802.11 DSSS PHY and defined to interoperate with existing IEEE 802.11 wireless networks operating at 1 and 2 Mbps.

The short preamble 14104 uses a 56-bit SYNC field to acquire the incoming signal, and transmits the preamble at 1 Mbps using DBPSK modulation and Barker word spreading. The PLCP header transmits at 2 Mbps using DQPSK and Barker word spreading (see FIG. 141). In this case, the PSDU is transmitted at 2, 5.5, or 11 Mbps as determined by the content in the signal field. The short preamble 14104 is an option in IEEE 802.11b and is useful for those networks where throughput efficiency and interoperability with existing IEEE 802.11 DSSS radios in not necessary. Because the short preamble radio may only interoperate with itself, a short preamble radio must support the long preamble 14102 to be IEEE 802.11b compliant.

SYNC: The receiver uses this field to acquire the incoming signal and synchronize the receiver's carrier tracking and timing prior to receiving the start of frame delimiter (SFD). The long preamble SYNC field is 128 bits in length, and contains a string of scrambled 1s. The scrambler seed bit pattern used to initialize the scrambler for the long preamble is 01101100. The short preamble SYNC field is 56 bits in length, and contains a string of scrambled 0s. The scrambler seed bit pattern used to initialize the scrambler for short preamble operation is 00011010. The short

preamble SYNC field may be used for networks where minimizing overhead and maximizing PSDU throughput is a consideration.

SFD: This field contains information marking the start of a PPDU frame. The SFD specified is common for all IEEE 802.11 DSSS and IEEE 802.11b long preamble radios. The following hexadecimal word is used: F3A0hex transmitted LSB first. For short preamble radios, the following hexadecimal word is used: 05CFhex transmitted LSB first.

Signal: The signal field defines which type of modulation must be used to receive the incoming PSDU. The binary value in this field is equal to the data rate multiplied by 100 kbit/s. The 1 Mbps data rate is used for long and short preamble implementations. The bit patterns in this field and the respective data rates are shown in Table 9.

Signal Field	Data Rate
00001010	1 Mbps (long preamble only)
00010100	2 Mbps
00111110	5.5 Mbps
01101110	11 Mbps

Table 9

Service: The service field uses 3 bits of the reserved 8 bits for IEEE 802.11b. Data bit (b2) determines whether the transmit frequency and symbol clocks use the same local oscillator. Data bit (b3) indicates whether complimentary code keying (CCK) or packet binary convolutional coding (PBCC) is used and data bit (b7) is a bit extension used in conjunction with the length field to calculate the duration of the PSDU in microseconds. This field is used for the long and short preamble frames.

Length: The length field is an unsigned 16-bit integer that indicates the number of microseconds necessary to transmit the PSDU. For any data rate over 8 Mbps, bit-7 of the service

field is used with the length field to determine the time in microseconds from the number of octets contained in the length field. A calculation is defined in IEEE 802.11b for determining the length in microseconds for CCK and PBCC as applied to both preambles. The MAC layer uses this field to determine the end of a PPDU frame.

CRC: The CRC field contains the results of a calculated frame check sequence from the sending station. The calculation is performed prior to data scrambling for the long and short preamble. A CCITT CRC-16 error detection algorithm is used to protect the signal, service, and length fields. The CRC-16 algorithm is represented by the following polynomial: $G(x) = x^{16} + x^{12} + x^5 + 1$. The receiver performs the calculation on the incoming Signal, Service and Length fields, and compares the results against the transmitted value. If an error is detected, the receiver's MAC makes the decision whether incoming PSDU should be terminated.

6.7.2.2 High Rate Data Scrambling

All information bits transmitted by the DSSS PMD are scrambled using a self-synchronizing 7-bit polynomial. The scrambling polynomial for the DSSS PHY is: $G(z) = z^{-7} + z^{-4} + 1$. Scrambling is used to randomize the long and short preamble data in the SYNC field of the PLCP and for data patterns which contain long strings of binary 1s or 0s. The receiver can descramble the information bits without prior knowledge from the sending station. The scrambler initialization bit patterns are represented as (00011010) for the short preamble and (01101100) for the long preamble.

6.7.2.3 IEEE 802.11 High Rate Operating Channels

The HR/DSSS PHY uses the same frequency channels as defined for the IEEE 802.11 direct sequence PHY. The channel center frequencies are spaced 25 MHZ apart to allow multiple WLAN systems to operate simultaneously in the same area without interfering with each other. An example of a typical channel arrangement for non-interfering channels for North America is illustrated in FIG.

142. In Europe, the channels 1 (2.412 GHz), 7 (2.442 GHz), and 13 (2.472 GHz) are used to form three non-interfering networks.

6.7.2.4 IEEE 802.11 DSSS High Rate Modulation and Data Rates

There are four modulation formats and data rates defined in IEEE 802.11b. The data rates include the basic rate, the extended rate, and enhanced rate. The basic rate is defined as 1 Mbps modulated with DBPSK, and the extended rate is defined as 2 Mbps DQPSK modulated. The 11-bit Barker word is used as the spreading format for the basic and extended rate as described for the DSSS PHY herein. The enhanced rate is defined to operate at 5.5 Mbps and 11 Mbps using CCK modulation and packet binary convolutional coding (PBCC). PBCC is an option in the standard for networks requiring enhanced performance. Frequency agility is further option defined in IEEE 802.11b. As with the 1 and 2 Mbps DSSS PHY, this option enables existing IEEE 802.11 FHSS 1 Mbps networks to be interoperable with 11 Mbps CCK high rate networks. The PBCC and frequency agility option are further described below.

6.7.2.4.1 Complementary Code Keying (CCK) Modulation

In July of 1998, the IEEE 802.11 Working Group adopted CCK as the basis for the high rate extension to deliver PSDU frames at speeds of 5.5 Mbps and 11 Mbps. CCK was adopted because it provides for interoperability with existing IEEE 802.11 1 and 2 Mbps systems by maintaining the same bandwidth and incorporating the existing DSSS PHY PLCP preamble and header.

CCK is a variation on M-ary orthogonal keying modulation and is based on an in-phase (I) and quadrature (Q) architecture using complex symbols. CCK allows for multichannel operation in the 2.4 GHz band by using the existing 1 and 2 Mbps DSSS channelization scheme. CCK uses 8 complex chips in each spreading code word. Each chip can assume one of four phases (QPSK). CCK uses 64 base spreading code words out of a possible set of 65536 (i.e., $65536\text{-}4^3$). Base

spreading codes were chosen with beneficial autocorrelation and crosscorrelation properties. The CCK modulator chooses one of M unique for transmission of the scrambled PSDU. CCK uses one vector from a set of 64 complex quadrature phase shift keying (QPSK) vectors for the symbol and thereby modulates 6 bits (one of 64) on each spreading code symbol. An exemplary block diagram for a CCK modulator is shown in FIG. 143. Each spreading code is 8 complex chips in length. CCK uses a complex set of Walsh/Hadamard functions known as complementary codes. Refer to IEEE 802.11b for the equation used to derive the set of code words. There are four phase terms in the CCK equation. One of the terms modulates all of the chips, and is used for the QPSK rotation of entire code vector. The others modulate every odd chip, every odd pair of chips and every odd quad of chips. To minimize DC offsets, the 4th and 7th terms in the equation are rotated by 180 degrees with a cover sequence. As with the IEEE 802.11 DSSS PHY, the phase rotation for CCK is counterclockwise. To insure that the modulation has the same bandwidth as the legacy IEEE 802.11 DSSS PHY, the chipping rate is kept at 11 Mbps while the symbol rate is increased to 1.375 Mbps. The spreading rate remains constant while the data rate changes, and the CCK spectrum is the same as the legacy IEEE 802.11 waveform.

For 5.5 Mbps transmission, the scrambled binary bits of the PSDU are grouped into 4-bit nibbles, where two of the bits select the spreading function while the remaining two bits QPSK modulate the symbol, as illustrated in FIG. 144A. The spreading sequence DQPSK modulates the carrier by driving the I and Q modulators. For 11 Mbps operation, the incoming scrambled PSDU binary bits are grouped into 2 and 6 bits, as illustrated in FIG. 144B. The 6 bits are used to select (one of 64) complex vectors of 8 chips in length for the symbol and the other 2 bits DQPSK modulate the entire symbol. The transmit waveform is the same, and the chipping rate is maintained at 11 Mbps.

6.7.2.4.2 DSSS Packet Binary Convolutional Coding

Packet binary convolutional coding (PBCC) is an optional coding scheme defined in IEEE 802.11b. The coding option uses a 64-state binary convolutional code (BCC), rate R = ½ code, and a cover sequence. An exemplary PBCC modulator is illustrated in FIG. 145A. The HR/DSSS PMD uses PBCC to transmit the PPDU. To ensure that the PPDU frame is properly decoded at the receiver, the memory of the BCC encoder 14502 is cleared at the beginning and at the end of a frame. A cover sequence is used to map the QPSK symbols. The cover sequence is initialized with a 16-bit pattern (0011001110001011) to produce a 256-bit cover sequence, which selects the QPSK symbols. Binary phase shift keying (BPSK) is used for 5.5 Mbps, and QPSK for 11 Mbps. For QPSK, each pair of output bits from the BCC is used to generate one symbol. For BPSK, each pair of bits produces two symbols. The result is one bit per symbol for QPSK and ½ bit per symbol for BPSK. Refer to IEEE 802.11b for the equation used for the cover sequence generator 14504.

6.7.2.4.3 Frequency Hopped Spread Spectrum (FHSS) Interoperability

A channel agility option is defined in IEEE 802.11b which allows IEEE 802.11 FHSS 1 and 2 Mbps networks to interoperate with HR/DSSS 11 Mbps WLANs. Both non-overlapping and overlapping high rate channels are supported. The non-overlapping channels allow WLAN systems to operate simultaneously in the same area without interfering with each other. In North America, channels 1, 6, and 11 are specified for non-overlapping networks, and in Europe (excluding France and Spain) channels 1, 7, and 13 are specified as such. Two sets of hopping sequences are defined for worldwide operation. For more details on the hop patterns, refer to IEEE 802.11b.

6.7.2.5 *HR/DSSS PMD Incorporating Universal Frequency Translation Technology*

In embodiments, the HR/DSSS PMD may incorporate universal frequency translation technology to provide for modulation/de-modulation and frequency translation of WLAN station signals. For instance, the HR/DSSS PMD may comprise one or more UFT modules, such as UFT module 12810 of FIG. 128B, that provide for these functions. Furthermore, the HR/DSSS PMD may comprise one or more UFU modules such as UFU module 12812 of FIG. 128C, and/or one or more UFD modules such as UFD module 12814 of FIG. 128C, to provide for modulation/de-modulation and frequency translation of WLAN station signals. The HR/DSSS PMD of the present invention, using techniques of universal frequency translation, transmits and receives signals modulated according to DBPSK, DQPSK, CCK, and PBCC modulation schemes. Further specifications for these transmitted and received signals are provided above.

Embodiments for HR/DSSS PMD transmitters and receivers incorporating universal frequency translation technology are provided below. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the HR/DSSS PMD as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software, or any combination thereof. The invention is intended and adapted to include such alternate embodiments.

6.7.2.5.1 *Transmit HR/DSSS PMD Incorporating Universal Frequency Translation*

FIG. 143A illustrates a transmit HR/DSSS PMD 14300, according to an embodiment of the present invention. Transmit HR/DSSS PMD 14300 of the present invention comprises at least one UFT module 12810 for frequency translation/modulation/demodulation of WLAN station signals.

As described above, the transmit HR/DSSS PMD 14300 transmits WLAN signals according to DBPSK, DQPSK, CCK, and PBCC modulation schemes. For instance, in the case of a long preamble, transmit HR/DSSS PMD 14300 transmits the PLCP preamble and PLCP header at 1 Mbps according to DBPSK, and the PSDU is sent at either 1 Mbps DBPSK, 2 Mbps DQPSK, or 5.5 or 11 Mbps CCK or PBCC, depending on the content in the signal field and service field. In the case of a short preamble, transmit HR/DSSS PMD 14300 transmits the PLCP preamble at 1 Mbps using DBPSK, the PLCP header at 2 Mbps using DQPSK, and the PSDU is sent at either 2, 5.5, or 11 Mbps, depending on the content in the signal field.

Transmission of WLAN signals according to DBPSK and DQPSK modulation schemes are described in detail in Section 6.6.2.6.1 above in reference to transmit DSSS PMD 12900. The structure and operation of transmit DSSS PMD 12900 is applicable to transmit HR/DSSS PMD 14300, and is hence considered incorporated in transmit HR/DSSS PMD 14300. Refer to Section 6.6.2.6.1 above for detailed description of transmission of DBPSK and DQPSK modulated signals by transmit HR/DSSS PMD 14300. The transmission of CCK and PBCC modulated signal is described below.

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6.7.2.5.1.1 Transmitter Embodiments for CCK Modulation

As shown in FIG. 143B, transmit HR/DSSS PMD 14300 comprises a CCK modulator 14324, according to embodiments of the present invention. CCK modulator 14324 modulates WLAN station signals according to CCK modulation techniques. CCK modulator 14324 comprises a scrambler 14302, a data multiplexer 14304, a complex code selector module 14306, and a DQPSK modulation transmitter 14308. The structure and operation of transmit HR/DSSS PMD 14300 in a CCK modulation mode will be described as follows, and is further described elsewhere herein.

Scrambler 14302 receives a PSDU signal 14310. In embodiments, PSDU signal 14310 may comprise one or more PPDU frames, and/or PPDU frame portions, such as the PSDU, to be

modulated according to CCK modulation. Alternatively, the HR/DSSS PMD PSDU may be modulated according to any of the modulation schemes described herein.

Scrambler 14302 scrambles the PSDU signal 14310, and outputs a scrambled PSDU signal 14312. The design and use of a scrambler 14302 is well known to those skilled in the relevant art(s). A suitable scrambler 14302 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Data multiplexor 14304 receives scrambled PSDU signal 14312. Data multiplexor 14304 multiplexes scrambled PSDU signal 14312, and outputs first multiplexed output signal 14314 and second multiplexed output signal 14316. In a 5.5 Mbps embodiment, first multiplexed output signal 14314 is 2 bits wide. In an 11 Mbps embodiment, first multiplexed signal 14314 is 6 bits wide. Second multiplexed output signal 14316 is 2 bits wide. The design and use of a data multiplexor 14304 is well known to those skilled in the relevant art(s). A suitable data multiplexor 14304 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Complex code selector module 14306 receives first multiplexed output signal 14314. Complex code selector module 14306 selects a spreading code using first multiplexed output signal 14314. In a 5.5 Mbps embodiment, the spreading code is selected from 4 possible code words. In an 11 Mbps embodiment, the spreading code is selected from 64 possible code words. Complex code selector module 14306 outputs spreading code 14318. The design and use of a complex code selector module 14306 is well known to those skilled in the relevant art(s). A suitable complex code selector module 14306 may be designed and implemented in software, firmware, hardware, and any combination thereof.

DQPSK modulation transmitter 14308 receives second multiplexed signal 14316 and spreading code 14318. DQPSK modulation transmitter 14308 modulates spreading code 14318 with second multiplexed signal 14316 according to the technique of DQPSK modulation.

In an embodiment, DQPSK modulator operates similarly to modulator 12978 of FIG. 129I, and comprises a transmitter such as I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300,

which combines and frequency up-converts these signals to a transmitted modulated signal. The resulting transmitted modulated signal may be transmitted by an antenna. Also refer to the DQPSK modulation transmitter configurations of FIGS. 129G-129I for further configurations for providing DQPSK modulation in transmitter 14308 of FIG. 143B.

In an alternate embodiment, DQPSK modulation transmitter 14308 outputs I data 14320 and Q data 14320, as shown in FIG. 129I, which are input to a transmitter such as I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300. I/Q transmitter 7402, 7608, 7618, 7702, 7802, 8000, 8200, 8300 combines and frequency up-converts these signals to a transmitted modulated signal, which may be transmitted by an antenna. Alternate embodiments for CCK modulator 14324 (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.7.2.5.1.2 Transmitter Embodiments for PBCC Modulation

As shown in FIG. 145A, transmit HR/DSSS PMD 14300 comprises a PBCC modulator 14500, according to embodiments of the present invention. PBCC modulator 14500 modulates WLAN station signals according to PBCC modulation techniques. PBCC modulator 14500 comprises a binary convolutional code encoder 14502, a cover code sequence generator 14504, a scrambler 14506, a QPSK cover code map module 14508, and a QPSK modulation transmitter 14510. The structure and operation of transmit HR/DSSS PMD 14300 in a PBCC modulation mode will be described as follows, and is further described elsewhere herein.

Scrambler 14506 receives PPDU signal 14512. In embodiments, PPDU signal 14512 may comprise one or more PPDU frames, and/or PPDU frame portions, such as the PSDU, the PLCP preamble, and the PLCP header, to be modulated according to PBCC modulation. Alternatively, the HR/DSSS PMD PPDU may be modulated according to any of the modulation schemes described herein.

Scrambler 14506 scrambles PPDU signal 14512, and outputs scrambled PPDU signal 14512. The design and use of a scrambler 14506 is well known to those skilled in the relevant art(s). A suitable scrambler 14506 may be designed and implemented in software, firmware, hardware, and any combination thereof, or it may be purchased "off the shelf."

Binary convolutional code encoder 14502 receives scrambled PPDU signal 14512. Binary convolutional code encoder 14502 encodes scrambled PPDU signal 14512, and outputs encoded signal 14512. The design and use of a binary convolutional code encoder 14502 is well known to those skilled in the relevant art(s). A suitable binary convolutional code encoder 14502 may be designed and implemented in software, firmware, hardware, and any combination thereof.

Cover code sequence generator 14504 receives 16-bit cover code seed 14520. Cover code sequence generator 14504 generates cover code sequence 14518. The design and use of a cover code sequence generator 14504 is well known to those skilled in the relevant art(s). A suitable cover code sequence generator 14504 may be designed and implemented in software, firmware, hardware, and any combination thereof.

QPSK cover code map module 14508 receives encoded signal 14512 and cover code sequence 14518. QPSK cover code map module 14508 maps encoded signal 14512 via cover sequence 14518, and outputs mapped I signal 14522 and mapped Q signal 14524. A suitable QPSK cover code map module 14508 may be designed and implemented in software, firmware, hardware, and any combination thereof, as would be understood by persons skilled in the relevant art(s) from the teachings herein.

QPSK modulation transmitter 14510 receives mapped I signal 14522 and mapped Q signal 14524. QPSK modulation transmitter 14510 modulates mapped I signal 14522 and mapped Q signal 14524 according to QPSK modulation, and outputs modulated output signal 14526. FIGS. 129G-129I illustrate exemplary DQPSK modulation transmitter configurations related to transmitter 12910 of FIG. 129A, according to embodiments of the invention. The DQPSK modulation transmitter configurations of FIGS. 129G-129I are adaptable to providing for QPSK modulation in transmitter 14510 of FIG. 145A, according to further embodiments of the present invention. For instance,

referring to FIG. 129G, in a QPSK modulation embodiment, DQPSK modulation transmitter 12978 may be adapted to a QPSK modulation transmitter. As a result, transmitted modulated signal 12924 is a QPSK modulated signal. Referring to FIG. 129H, in a QPSK modulation embodiment, first and second DBPSK modulators 12909 and 12980 may be adapted to first and second BPSK modulators, respectively. As a result, first and second DBPSK modulated signals 12901 and 12975 are BPSK modulated signals. Referring to FIG. 129I, in a QPSK modulation embodiment, first and second DBPSK modulators 12911 and 12913 are adapted to first and second BPSK modulators, respectively. As a result, first and second DBPSK modulated signals 12977 and 12979 are BPSK modulated signals.

Hence, the DQPSK modulation transmitter configurations of FIGS. 129G-129I may be referred to for exemplary QPSK modulation embodiments of QPSK modulation transmitter 14510. Refer to Section 6.6.2.6.1.3 for further description of the structure and operation of the DQPSK modulation transmitter configurations of FIGS. 129G-129I. Alternate QPSK modulation transmitter embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.7.2.5.2 Receiver HR/DSSS PMD Incorporating Universal Frequency Translation

FIG. 145B illustrates a receiver HR/DSSS PMD 14528, according to an embodiment of the present invention. Receiver HR/DSSS PMD 14528 of the present invention comprises at least one UFT module 12810 for frequency translation/modulation/demodulation of WLAN station signals.

As described above, receiver HR/DSSS PMD 14528 receives and demodulates WLAN signals modulated according to DBPSK, DQPSK, CCK, and PBCC modulation schemes. For example, receiver HR/DSSS PMD 14528 of the present invention demodulates the DBPSK-

modulated PLCP preamble, the DBPSK- or DQPSK-modulated PLCP header, and demodulates the DBPSK-, DQPSK-, CCK-, or PBCC-modulated PSDU.

Receivers for receiving WLAN signals modulated according to DBPSK and DQPSK modulation schemes are described in detail in Section 6.6.2.6.2 above in reference to receiver DSSS PMD 12902. The structure and operation of receiver DSSS PMD 12902 is applicable to receiver HR/DSSS PMD 14528, and is hence considered incorporated in receiver HR/DSSS PMD 14528. Refer to Section 6.6.2.6.2 above for detailed description of the reception of DBPSK and DQPSK modulated signals by receiver HR/DSSS PMD 14528.

As shown in FIG. 145C, receiver HR/DSSS PMD 14528 comprises a CCK demodulator 14530, according to embodiments of the present invention. CCK demodulator 14530 comprises at least one UFT module 12810. CCK demodulator 14530 demodulates CCK modulated WLAN station signals. As described above, CCK modulated WLAN station signals are generated in part by techniques including DQPSK/QPSK modulation. In embodiments, CCK demodulator 14530 incorporates the structure and operation of QPSK modulation receiver 12939 described above in Section 6.6.2.6.2 in regards to demodulation of DQPSK modulated signals. In further embodiments, CCK demodulator 14530 incorporates the structure and operation of QPSK/QAM modulation receiver 14098 described above in Section 6.7.1.5.2 in regards to demodulation of QPSK modulated signals. Refer to Sections 6.6.2.6.2 and 6.7.1.5.2 above for detailed description of the reception of DQPSK and QPSK modulated signals by receiver HR/DSSS PMD 14528.

As shown in FIG. 145D, receiver HR/DSSS PMD 14528 comprises a PBCC demodulator 14532, according to embodiments of the present invention. PBCC demodulator 14532 comprises at least one UFT module 12810. PBCC demodulator 14532 demodulates PBCC modulated WLAN station signals. As described above, PBCC modulated WLAN station signals are generated in part by techniques including DQPSK/QPSK modulation. In embodiments, PBCC demodulator 14532 incorporates the structure and operation of QPSK modulation receiver 12939 described above in Section 6.6.2.6.2 in regards to demodulation of DQPSK modulated signals. In further embodiments, PBCC demodulator 14532 incorporates the structure and operation of QPSK/QAM modulation

receiver 14098 described above in Section 6.7.1.5.2 in regards to demodulation of QPSK modulated signals. Refer to Sections 6.6.2.6.2 and 6.7.1.5.2 above for detailed description of the reception of DQPSK and QPSK modulated signals by receiver HR/DSSS PMD 14528.

Alternate embodiments for receiver HR/DSSS PMD 14528 will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

6.8 System Design Considerations for IEEE 802.11 WLANs

The IEEE 802.11 WLAN standard provides a number of physical layer options in terms of data rates, modulation types, and spreading spectrum techniques. Selecting the correct physical layer and MAC technologies for an application requires careful planning and detailed systems analysis for developing the optimal WLAN implementation. The following sections focus on a few key considerations when implementing a compliant IEEE 802.11 interoperable WLAN system.

6.8.1 The Medium

A difference between a "wired" and a RF WLAN is the radio communications link. While a radio communications link provides the freedom to move without the constraints of wires, the wired media has the luxury of a controlled propagation media. Wireless RF media may be difficult to control because the dynamics of the propagated signals over the media are constantly changing. IEEE 802.11 WLANs may suffer from this difficulty because the 2.4 GHz bands are shared with unlicensed users. Radio system designers need to have a thorough understanding of the RF medium to properly design 2.4 GHz and 5 GHz IEEE 802.11 WLAN systems, especially for networks operating at data rates greater than 2 Mbps. The RF communication media for home, enterprise, and manufacturing environments may be different. Multipath and path loss are issues to consider when designing an IEEE 802.11 WLAN system.

6.8.2 Multipath

Multipath is a performance concern for indoor IEEE 802.11 WLAN systems. Multipath may occur when the direct path 9402 of a transmitted signal is combined with paths 9404 and 9406 of a reflected signal, resulting in a corrupted signal at the receiver 9408, as shown in FIG. 94. The delay of a reflected signal is measured in nanoseconds (nsec), and is commonly known as delay spread. Delay spread is the parameter used to signify multipath. The amount of delay spread varies for indoor, home, office, and manufacturing environments, as shown in Table 10. Surfaces of furniture, elevator shafts, walls, factory machinery, metal constructed buildings, and other objects may contribute to the amount of delay spread in a given environment.

Environment	Delay Spread
Home	<50 nsec
Office	~100 nsec
Manufacturing floor	200-300 nsec

Table 10

The channel impulse response is a way to illustrate the amount of multipath dispersion. For example, the amount of delay spread in an office environment may be approximately 100 nsec, as shown in FIG. 95. Typically, energy reflected by wall surfaces causes the impulse response to have energy on the leading edge before the peak. The leading energy is called the precursor energy. The amount of precursor energy differs from one environment to the next. The processing required to correct for the precursor energy is more complex than is required for the trailing edge energy. The symbol period on the x-axis of the graph in FIG. 95 is equal to the length of the 8 chip CCK code word. The 11 chip barker code is only 3 chips longer.

RAKE processing and equalization are two methods used to process and resolve delay spread. A RAKE receiver is a well-known architecture used to remove delay spreads on the order of 100 nsec. The RAKE is structured as a bank of correlators (fingers) with weighed delays, and a combiner. Equalization is an alternate architecture that may be used to correct delay spreads greater than 100 nsec. Multipath causes the signals from the previous symbol to interfere with the signals of the next. This is known as intersymbol interference (ISI). As with ISI, interchip interference (ICI) results when the signals of the previous chip interfere with the signals of the next chip. ISI and ICI are issues for higher data rate systems because the symbol and chip periods are shorter. This is the case for IEEE 802.11a and IEEE 802.11b. Equalization may correct for ISI and ICI. An equalizer is a multi-tapped delay line, which subtracts a delayed and attenuated signal from the actual received signal. However, for environments where delay spreads are greater than 200 nsec, more complex signal processing may be necessary. RAKE processing combined with ISI and ICI equalization is commonly implemented to resolve multipath dispersions of this magnitude.

6.8.3 Multipath Channel Model

In an environment where performance measurements of the same radio are used, in the same location, the results may not agree. This may be due to the changing position of people in the room and slight changes in the environment, which can produce significant changes in the signal power at the radio receiver. A consistent channel model is required to allow comparison of different WLAN systems and to provide consistent results. The IEEE 802.11 Working Group adopted the following channel model as the baseline for predicting multipath for modulations used in IEEE 802.11a (5 GHz) and IEEE 802.11b (2.4 GHz). This model is useful for software simulations predicting performance results for a given implementation. The channel impulse response illustrated in FIG. 96 is composed of complex samples with random uniformly distributed phase and Rayleigh distributed magnitude with average power decaying exponentially.

The mathematical model for the channel is provided as follows:

$$h_k = N\left(0, \frac{1}{2}\sigma_k^2\right) + jN\left(0, \frac{1}{2}\sigma_k^2\right)$$

$$\sigma_k^2 = \sigma_0^2 e^{-kT_s / T_{RMS}}$$

$$\sigma_0^2 = 1 - e^{-T_S / T_{RMS}}$$

Where $N\left(0, \frac{1}{2}\sigma_k^2\right)$ is a zero mean Gaussian random variable with variance $\frac{1}{2}\sigma_k^2$ produced by generating an N(0, 1) and multiplying it by $\sigma_k / \sqrt{2}$, and $\sigma_0^2 = 1 - e^{-T_s/T_{RMS}}$ is chosen so that the condition $\sigma_k^2 = 1$ I is satisfied to ensure same average received power.

Let T_S be the sampling period, and let T_{RMS} be the delay spread of the channel. The performance assessment shall be no longer than the smaller of 1/(signal bandwidth) or $T_{RMS}/2$. The number of samples to be taken in the impulse response should ensure sufficient decay of the impulse response tail, e.g. $k_{max} = 10 \times T_{RMS}/T_S$.

6.8.4 Path Loss in a WLAN System

Another key consideration is the issue of operating range relative to path loss. This consideration plays an important role in determining the size of overlapping WLAN cells and distribution of APs. Path loss calculations are equally important for determining a radio's receiver sensitivity, transmitting power level, and signal to noise ratio (SNR) requirements. As a radio transmits signals to other receivers in a given area, the signal is attenuated as a square of the distance (D). The distance D is the radius of a WLAN cell 9700, as shown in FIG. 97. FIG. 98 illustrates a graph and equations related to path loss. The wavelength (lambda) is the ratio between the speed of light and the signal frequency. As the receiver moves away from the transmitter, the receiver's

signal power decays until it reaches the receiver's noise floor, at which time the bit error rate becomes unacceptable. For indoor applications beyond 20 feet, propagation losses increase at about 30 dB per 100 feet. This may occur because of a combination of attenuation by walls, ceilings, and furniture. Each wall constructed with sheet rock and wood typically attenuates the signal by 6 dB, while walls constructed with cement block attenuate the signal by 4 dB. However, additional losses may occur depending on the fading characteristics of the operating environment, which is further described in the following section. The same path loss principles apply for all frequency bands. However, as the operating frequency increases from 2.4 GHz to 5 GHz, for example, an additional path loss of 5-10 dB occurs. This results in a smaller cell radius, and may require additional overlapping cells and APs to guarantee operation in the same area as a system operating at 2.4 GHz.

6.8.5 Multipath Fading

Another key consideration is the path loss due to multipath fading. Multipath fading occurs when the reflected signal paths refract off people, furniture, windows, and walls, and scatter the transmitted signal. For example, moving the receiver away from the transmitter by a small distance, even just a few inches, may produce an additional loss of signal power on the order of 20 dB or more. Multipath fading is viewed as two separate factors, and is described as probability distribution functions. The first factor is a characteristic known as log normal fading. These are coefficient products which result when the signal reflects off surfaces and propagates to the receiver. As the signal coefficient products propagate to the receiver, they are summed together with the direct path where they may cancel each other, possibly causing significant attention of the transmitted signal. This is the second factor, known as Rayleigh fading. As previously discussed herein, RAKE architectures and equalization may be used to correct for these effects.

6.8.6 Es/No vs BER Performance

System performance tradeoffs are often made in the decision process when selecting a modulation type and data rate. System tradeoffs in terms of receiver sensitivity, range, and transmit power become very important for developing low cost implementations, especially for higher rate 2.4 GHz IEEE 802.11b systems. FIG. 99 illustrates a graph providing a comparison of the theoretical Es/No vs Bit Error Rate (BER) curves for uncoded QPSK, PBCC 5.5-11 Mbps, CCK 5.5-11 Mbps, and Barker 1 and 2 Mbps. The theoretical curves include additive white Gaussian (AWG) noise in the channel. These curves are provided as a guide to assess the performance for a complete system implementing CCK and PBCC. However, to obtain a better understanding of the overall systems performance, other factors such as multipath, signal fading, carrier phase noise, noise figure, and other implementation losses should be considered in the link budget as part of the systems analysis.

6.8.7 Data Rate vs Aggregate Throughput

The IEEE 802.11 standard defines data rate in terms of symbol rate, or available bit rate. The PPDU data is modulated and transmitted over the RF or IR medium at this rate. This rate is often confused with the aggregate data throughput. The aggregate data rate takes into account overhead associated with protocol frame structure, collisions, and implementation processing delays. The implementation processing delays are associated with frames processed by mobile stations and APs. Simulations may be run in software to estimate the aggregate throughput of the protocol and benchmarked against compliant IEEE 802.11 WLAN systems. However, calculating the aggregate throughput can be complex because there are a number of detailed variables to consider. The protocol overhead includes parameters such as RTS, CTS, ACK frames, (SIF, DIFs, PIFs) interframe space timing, beacon periods and random back-off periods, estimated collisions, PPDU frame size, and RF propagation delays. An useful estimate of the average aggregate throughput of an IEEE

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802.11 wireless network is 75% of the data rate for DCF operation, and 85% of the data rate for PCF operation.

6.8.8 WLAN Installation and Site Survey

Many installations begin with a site survey. A site survey may serve a number of purposes. First, the survey may be used to determine the maximum operating range between an AP (fixed location) and mobile stations for a specified transmit RF power level. Second, a survey may help to identify holes in coverage due to multipath, interference sources, and neighboring existing WLAN installations. Third, a survey may be used in cell planning of overlapping BSAs, and for layout of APs, to provide them with hardwired access to existing wired Ethernet LAN infrastructures.

Many equipment manufactures have tests built into their products to conduct such surveys. PC laptops having IEEE 802.11 WLAN adaptor cards, with embedded software tools, are commonly used. In some cases, a spectrum analyzer with special directional antennas may be used to measure path loss through walls and other obstructions, and to pinpoint and identify interference sources. Some of the tests include bit error rate (BER) and packet error rate (PER), and link quality measurements as a function of range. Typically, the tests are recorded using a pair of WLAN adaptors; the first WLAN adaptor is set up in a fixed location, and the second WLAN adaptor is set up as a mobile station. Each environment is different, and the number of APs required for a given installation generally depends upon the presence of holes in the coverage area due to multipath, and signal attenuation through walls, ceilings, and floors. However, on average, for indoor operation, the maximum operating distance between a mobile station and an AP operating at a 2.4 GHz frequency, transmitting at an RF transmit power of +20 dBm (100 mW) at data rates of 1 and 2 Mbps, is approximately 400 feet, and is approximately100 feet at 11 Mbps.

6.8.9 Interference in the 2.4 GHz Frequency Band

A microwave oven used in household and commercial kitchens is frequently the main interference source in the 2.4 GHz unlicensed frequency band. The magnetron tubes used in microwave ovens radiate a continuous-wave-like (CW-like) interference that sweeps over tens of megahertz (MHZ) of the 2.4-2.483 GHz band during the positive half cycle of ac line voltage. A microwave oven's EIRP has a maximum generally ranging between 16 and 33 dBm. The power cycle frequency is 50 Hz 20 msec or 60 Hz 16 msec, depending upon the geographical location. In North America, the ac line frequency is 60 Hz, and a microwave oven's magnetron pulses on for 8 msec and off for 8 msec. The maximum packet length defined in the IEEE 802.11 protocol was designed to operate between the 8 msec pulses of microwave energy.

Other sources of interference include neighboring in-band radios. Two types of interference are considered here: The first type is co-channel interference, which is induced by radios from adjacent cells that are on the same channel frequency. Proper cell planning of the channel frequency and hopping patterns, and careful layout of the APs can minimize this interference. The second type of interference is due to systems such as neighboring DSSS and FHSS WLAN networks. Three mechanisms are built into the standard to assist in minimizing the amount of interference. The first mechanism is the clear channel assessment, where the MAC layer protocol provides a method of collision avoidance. The second mechanism is processing gain, which provides some protection from FHSS radios, whose spectrum appears as narrowband interferers. The third mechanism is hop patterns. There is sufficient frequency spacing between pseudo-random hops to minimize the interference due to neighboring DSSS channels. To some degree, legacy 2.4 GHz IEEE 802.11-compliant FHSS and DSSS systems and IEEE 802.11b high-rate WLAN systems may coexist. However, careful cell planning will assist in minimizing the amount of interference a system will experience, especially at the outer fringe of the cell.

6.8.10 Antenna Diversity

Historically antenna diversity has been an effective low-cost alternative solution used to combat and mitigate the effects of multipath and delay spread in WLAN radio receivers. It is relatively easy to implement in the mobile stations and APs, and does not require the signal processing hardware used in other diversity techniques. The objective of antenna diversity is to space the antennas apart from each other to minimize the effects of the uncorrelated multipath at the receiver. By spacing the antennas far apart, the receiver may select and demodulate the larger of the two signals. For 2.4 GHz IEEE 802.11 implementations, the bit length of the preamble sync fields was selected based on these criteria. The antennas are typically spaced anywhere from 0.251 to several lambdas (wavelengths) apart. The amount of separation depends upon the amount of delay-spread tolerance required for the system to operate in a given operating environment. Adding antenna diversity may improve the packet error rate (PER) performance of a wireless link by 2 to 1, as well as improve the availability of the link. There are a number of 2.4 GHz antennas available with different configurations. Patch antennas are commonly used in the mobile client PCMCIA implementations, due at least in part to cost and size constraints. On the other hand, omni-directional antennas may be used at the AP because they provide reasonably optimal antenna coverage. Although antenna diversity is an option in the standard, at a minimum, antenna diversity should always be considered at the AP, as shown in FIG. 100. This form of diversity will assist in minimizing the risk of packet loss due to multipath and interference, and help to ensure reasonably optimal throughput performance in a system.

7. Appendix

The attached Appendix contained in FIGS. 146 to 212, which forms part of this patent application, includes schematics of an integrated circuit implementation example of the present invention. This example embodiment is provided solely for illustrative purposes, and is not limiting.

Other embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings herein.

8. Conclusions

Example implementations of the systems and components of the invention have been described herein. As noted elsewhere, these example implementations have been described for illustrative purposes only, and are not limiting. Other implementation embodiments are possible and covered by the invention, such as but not limited to software and software/hardware implementations of the systems and components of the invention. Such implementation embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, various WLAN components have been described herein as being implemented using various UFT, UFU, and/or UFD, etc., embodiments. These embodiments have been described for illustrative purposes only, and are not limiting. Such WLAN components can alternatively be implements using other frequency translation embodiments described herein, and/or using equivalents thereof, as will be apparent to persons skilled in the relevant arts based on the teachings contained herein.

Thus, while various application embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.